

EDN

Power semiconductors

Fiber-optic couplers

High-speed comparators

Designer's Guide to:
Simulation and test vectors

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Development tools
work wonders for
32-bit- μ P systems

now climbing to the top.

Intersil's accomplishments in data acquisition prove that no one comes close to us in the range and quality of CMOS data acquisition devices we offer.

And the story's the same whether you're talking data conversion, linear devices, analog switches, digital controllers, micro-peripherals or high-reliability.

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- to develop precision A/D and D/A data conversion products.

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Intersil puts you first.

All of our firsts—and we've named just a few—are worthless if they don't help you do your job better.

And they do. Here's a short list of the things you can do with our broad range of data acquisition products:

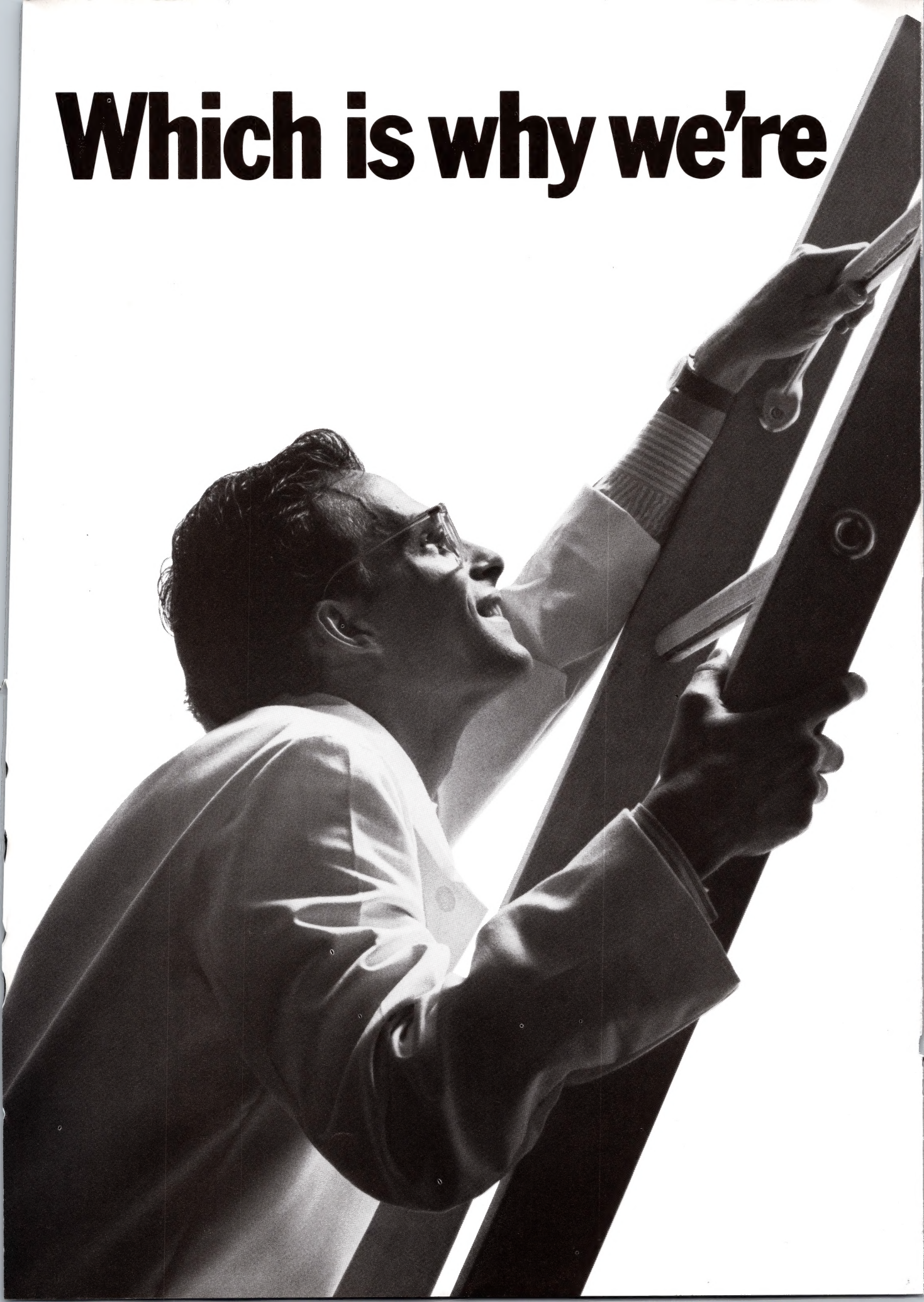
- Solve your difficult design problems. With Intersil products, you've got a complete set of "building blocks."
- Count on us. Of the last 25 data acquisition products we've introduced, 21 are now second-sourced. (As of February 21, 1985.)
- Think of us when you need total product solutions from one supplier. Whether it's linear products or analog solutions on a chip.
- Look to us for technological leadership. Other chip-makers do! That's why their copies of our industry standards are the sincerest form of flattery.
- Know we'll be there. It's taken nearly two decades of innovation and perspiration to get us to the top, and we intend to stay here. That's why we've invested \$20 million in new production facilities, including state-of-the-art wafer fab and assembly.

For more information about Intersil's fine line of data acquisition products, call: 800-626-2001 ext. 428. Or write to: Intersil, Inc., Mail Stop R1-26, 10600 Ridgeview Court, Cupertino, CA 95014

Signal processing is our business. Excellence is our goal. That's why we're climbing to the top. And why we can say, with pride: GE stands for Great Engineering.



Which is why we're



**GE
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Great
Engineering
in data
acquisition:**

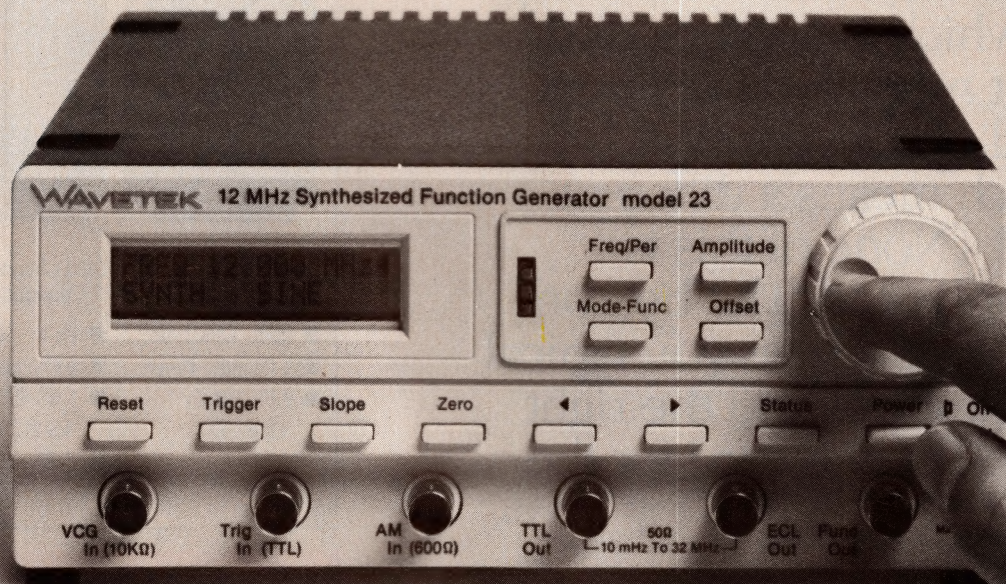
Take our low-priced synthesized function generator for a test spin.

You'll be amazed at how easily Model 23 can be controlled. Just push a button to select the parameter and turn the knob to increment or decrement the setting. A 16-character by 2-line display shows the value with 4-digit precision. Settings that can be displayed include frequency or period, function, offset and amplitude (in Vp-p, Vp, V RMS or dBm).

If you're more interested in performance than handling, Model 23 will keep you happy. It produces quartz-accurate waveforms from 0.01 Hz to 12 MHz, and the clock also provides accurate TTL or ECL outputs up to 32 MHz. Modes include AM, FM, trigger and gate.

Although the Model 23 is designed to be parked on a bench, it can be programmed via optional GPIB or RS232 interfaces.

The size is also impressive—like the \$1995 price, it's very small. To put your finger on the new Model 23, just contact Wavetek San Diego, P.O. Box 85265, 9045 Balboa Ave., San Diego, CA 92138. Phone (619) 279-2200; TWX (910) 335-2007.



And you need more than one way, because everyone's applications are different. Sometimes it's just a

Three different Z 80 multi-function CPU cards, because there's more than one way to make them talk.

Terminal-to-Printer conversation — which is one card.

Or it might be a long-distance conversation with a remote system 4000' away — which is another card.

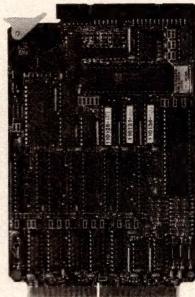
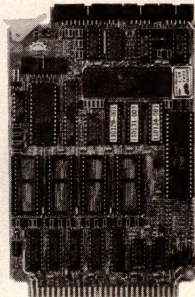
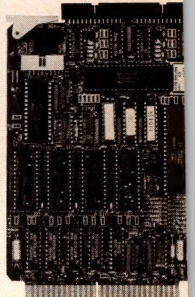
Or it might be a different kind of conversation — which means a different card. (None of this is complicated. The box on this page shows you typical applications and the right Z80 STD BUS card for the job.)

The card you pick depends on what you want to talk to what — and what about. We have a whole family of cards to pick from — so

whatever you're designing or managing, there's a Pro-Log card to make things work.

To order — call us for more

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Dual Channel Local Communications	Dual Channel Remote Communications	Terminal/Printer Communications
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On the cover: With the aid of props like in-circuit emulators, you can easily conjure up products that incorporate 32-bit μ Ps. See pg 106. (Photo courtesy National Semiconductor)

DESIGN FEATURES

Special Report: Development systems for 32-bit μ Ps 106

With the introduction of 32-bit μ Ps, a microprocessor development system will no longer be limited to a single-user host coupled to an in-circuit emulator. Now such tools can range from software development systems made from board-level products to high-speed bit-slice hardware-development equipment.

Follow design rules for optimum use of fast comparator IC 129

To fully exploit a high-speed comparator IC's capabilities, you must understand both the IC's innate attributes and the influences of the circuit environment surrounding the device.

Designer's Guide to: Simulation and test vectors—Part 1 153

To evaluate logic designs correctly, logic simulators require accurate input vectors. You must generate the appropriate vectors to verify your logic's functionality and to determine dynamic operation, performance margins, and critical timing constraints.

Design a simple dual-UART-based network 163

With a dual UART and some simple circuitry, you can easily design an inexpensive network. Each network station has identical interface hardware and software; you can expand the network's function to cover binary-file transfer and electronic mail.

MTBF values aid in predicting component failures 177

The concepts of reliability, failure rate and mean time between component failures are frequently misunderstood and misused. Although related, each represents a different aspect of a component's projected operating life.

Understand probe resistance to ensure accurate measurements 187

When you choose a probe for an oscilloscope measurement, consider the effects of the probe's resistance on your circuit. By selecting the right probe, you can avoid measurement errors.

Continued on page 7

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The Fluke 80TK. One innovation leads to another.

First there was the 70 Series, which set a new standard for low-cost, high-performance, Fluke-quality multimeters.

And now, another first. The Fluke 80TK K-type Thermocouple Converter. A temperature measurement device that adds instant temperature measurement capabilities to the 70 Series DMMs.

Or any DMM, for that matter.

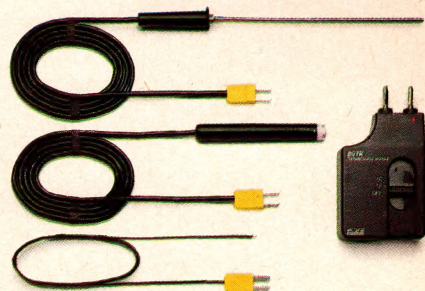
Feature for feature, the versatile 80TK is the most affordable unit of its kind. For quick comparison readings, it can measure °C or °F at the flick of a switch. It includes a built-in battery test. And the availability of 3 Fluke probes give you the flexibility to measure any

form of temperature, from freezer to furnace, with just one base unit.

No other thermocouple converter we know of offers DMM users so much for so little. Just \$59, including a general-purpose bead probe.

So even if you don't own a Fluke 70 Series multimeter, the 80TK will help the DMM you're now using measure up when things get hot. Or cold.

For more information, contact your local Fluke representative.



Surface, immersion and general-purpose probes with "mini" thermocouple connectors are available for the Fluke 80TK.

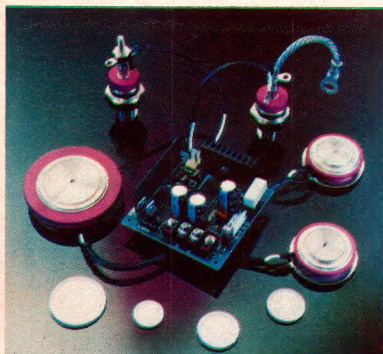
80TK SPECIFICATIONS

Temperature Measurement Range	
-50 to 1000°C	
-58 to 1832°F	
Battery Life: 1600 Hours (9V)	

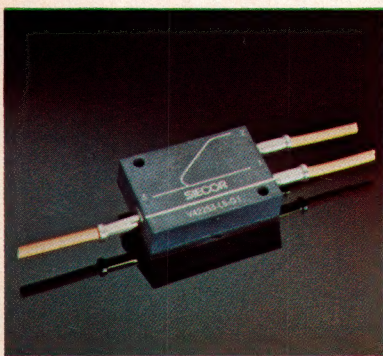
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Gate-turn-off thyristors are reducing the cost and complexity of equipment that employs power semiconductors. But although the GTOs minimize the number of power components in such equipment, the drive-circuit complexity increases (pg 61).



Once mere laboratory curiosities, fiber-optic couplers are now available off the shelf in a variety of configurations and technologies (pg 75).

TECHNOLOGY UPDATE

Gate-turn-off thyristors spec new current/voltage highs

61

Gate-turn-off (GTO) thyristors are replacing silicon controlled rectifiers as solid-state switches in high-frequency power-conversion equipment. GTO thyristors are now available with voltage ratings as high as 4.5 kV.

Multiple-access fiber-optic couplers enhance data-link performance

75

Multiport fiber-optic couplers (devices with three or more access points) can add flexibility and sophistication to your fiber-optic system and network designs: They allow for bidirectional transmissions; let you tap, split, and combine transmissions; and permit you to multiplex signals.

PRODUCT UPDATE

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DESIGN IDEAS

Circuit provides temperature compensation	193
PCM filter offers lowpass, bandpass options	194
Program provides gray/binary conversion	196
Vary frequency without changing duty cycle	199
Circuit measures capacitor's resistance	200

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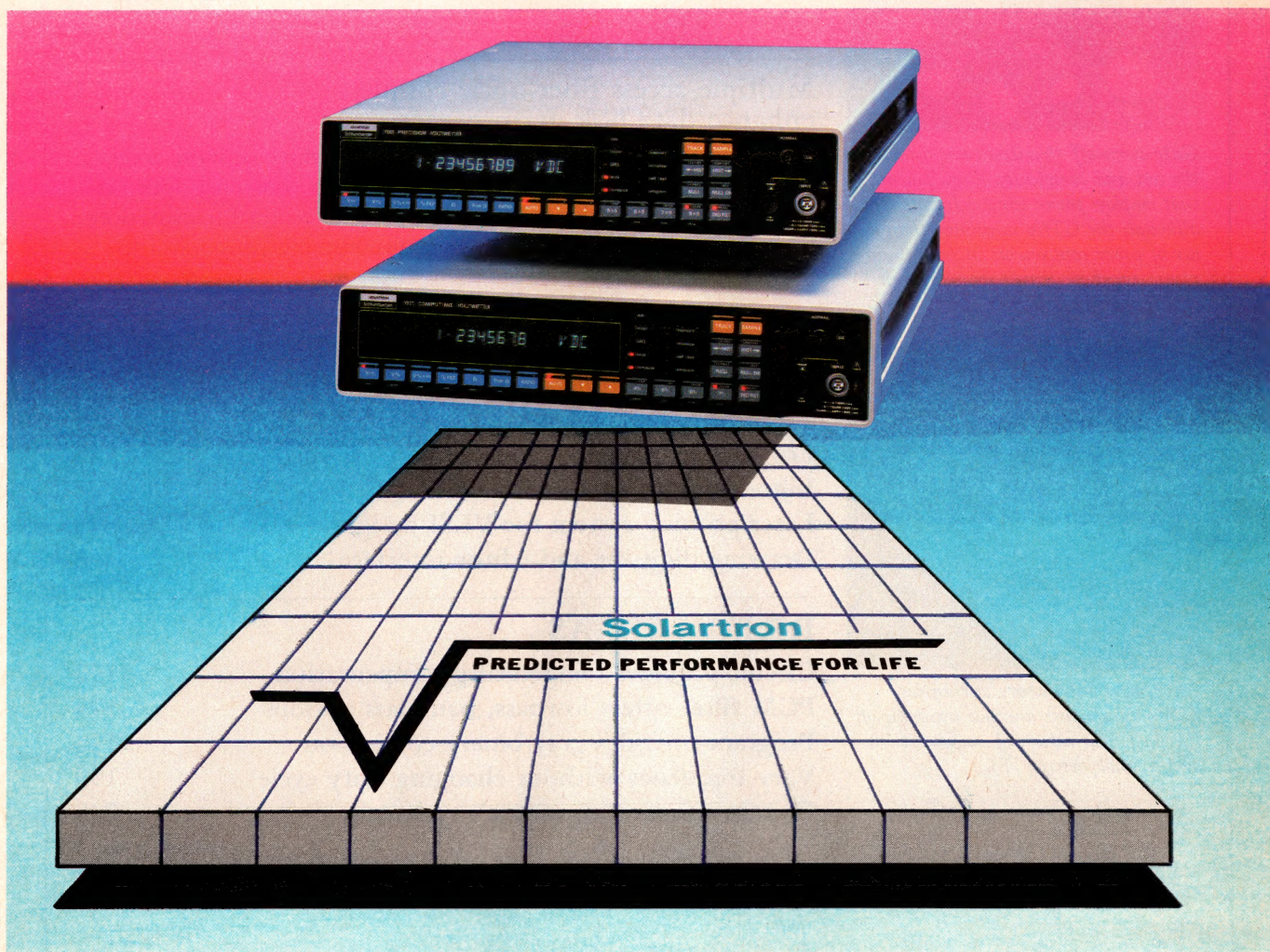
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Volts dc	10 nV to 1000V	1.2 ppm/24 hr. 11 ppm/1yr. 33 ppm/9yr	3 ppm/24hr. 20 ppm/1yr 66 ppm/9 yr.
Volts, true rms ac Ohms Transfer Accuracy Linearity	1μV to 750V 10Ω to 1000MΩ	150 ppm 1.5 ppm 0.4 ppm 0.3 ppm	150 ppm 1.5 ppm 1 ppm 0.5 ppm

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EDITORIAL

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Barely a decade ago, microprocessors were new and largely unknown. Then, in seemingly no time at all, μ Ps were everywhere. Now, only a decade later in time, but generations later in technology, 32-bit μ Ps are repeating some of the history written by their 4-, 8-, and 16-bit predecessors.

NEW PRODUCTS

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NSF research centers open with high hopes for innovative technology, better-trained EEs..... 257

LOOKING AHEAD

275

Voice/data terminal sales to reach \$650M in '87.... Motion-control market to double in Europe by '89.

DEPARTMENTS

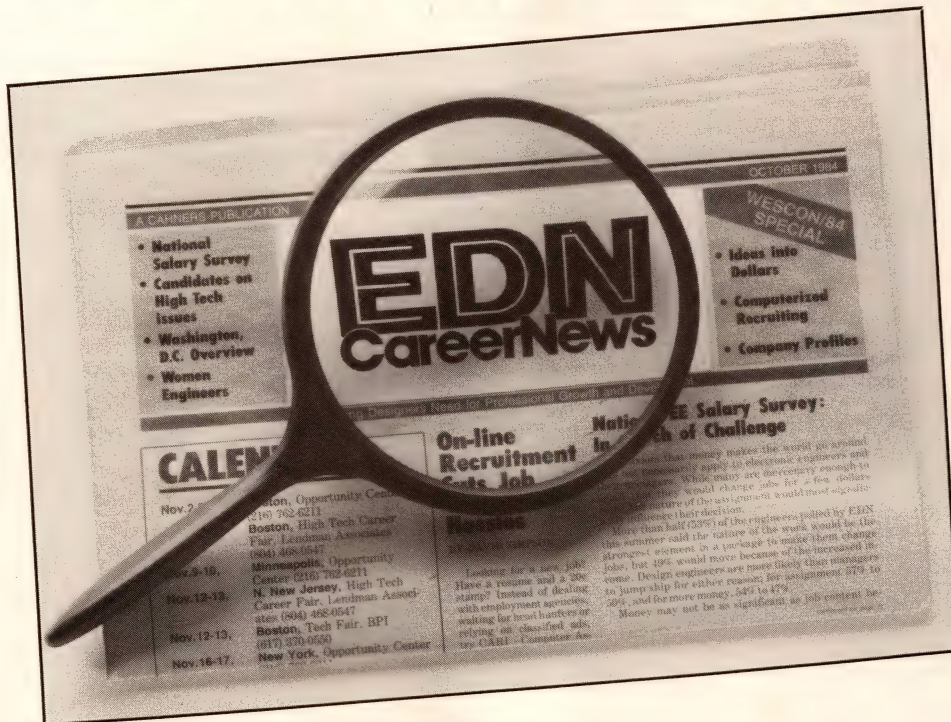
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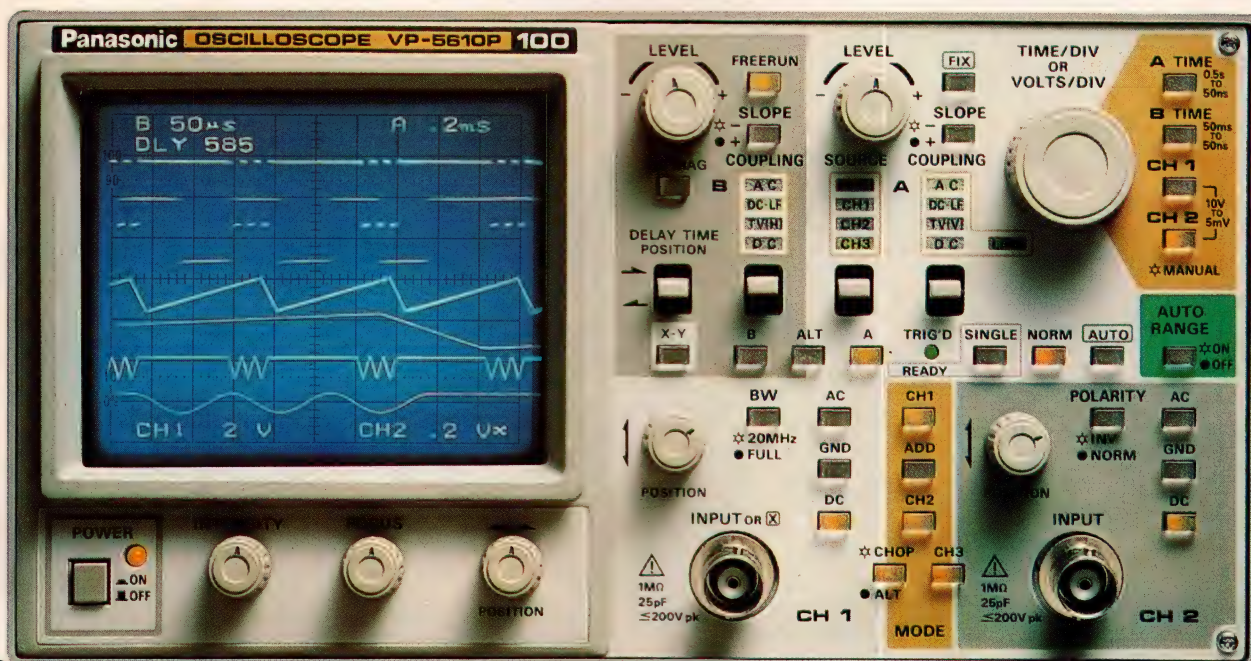
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If you're looking for a really compact oscilloscope that travels anywhere and operates anywhere (AC universal input from 90 to 250V and DC), look no further. Our VP-5610P, with its advanced circuit design technology, can rest on one hand and still get the job done for you. For extra functions you get Auto Ranging which automatically specifies sweep range and vertical sensitivity best suited for

an unknown or indefinite input signal. You also get a handy probe with GND reference. The probe has a built-in switch right at your finger-tips for starting the auto ranging function. This plus 3-trace, an alternate sweep function, auto fix, hold-off, a drift compensation circuit, digital readout and much more make this versatile model a super scope, especially if you're busy and need something portable.



194(W)×102(H) mm

★ This chart compares the necessary preparatory and measuring steps of a conventional oscilloscope (11 steps) to the advanced National/Panasonic VP-5610P (only 5 steps)

Measuring Made Easy:★	Conventional Oscilloscope	National/Panasonic VP-5610P
Preparations		
1. Turn on power, adjust intensity and focus	●	●
2. Adjust V position	●	
3. Set V range	●	
4. Specify trigger mode	●	
5. Specify sweep range	●	
Measuring		
6. Connect probe and apply to measurement point	●	●
7. Refine V range	●	
8. Adjust trigger slope	●	
9. Refine trigger	●	
10. Refine sweep range	●	
11. Read out waveform	●	
	11 steps	5 steps



National/Panasonic

Matsushita Electric Trading Co., Ltd., Industrial Electronics Section
P.O. Box 18, Trade Center, Tokyo 105, Japan Telex: 522-8771 "METOSK J"

CIRCLE NO 148



SERIES 32000 IS A TRADEMARK OF NATIONAL SEMICONDUCTOR CORPORATION.



"I can tell by the look on your face. You've been talking to marketing about the new system again."

"How're we going to do it if you have to create memory management and floating point units out of thin air?"

"That's not a problem—"

"On time and on budget?"

"We're going to use a complete 32-bit chip set—"

"We can't make a system out of data sheets. We need product, not promises."

"I'm talking about the Series 32000 family. It's real. It's here. I like it and the software people love it. What more do you want?"

"Can we start today?"

Today, only one 32-bit microprocessor gives you all the power you want, and all the parts you need.

If you're building an extraordinary new system, you can't do it with less than extraordinary components. And you certainly can't do it on time without floating point and memory management units.

Of all the available 32-bit microprocessors, only one delivers supermini performance from a chip set you can work with today. Series 32000™ is the world's most complete 32-bit microprocessor family, with CPU, MMU, FPU, TCU, ICU and DMA controllers in place right now.

So instead of creating essential components from scratch, start your design today with Series 32000, the complete 32-bit family.

For all the facts, write to:
Series 32000, MS 23-200
National Semiconductor
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090



**National
Semiconductor**
We're doing it.

THE SUPERMINI ON A CHIP

CIRCLE NO 14

The image is a full-page advertisement featuring a dense grid of brown plastic storage bins. The bins are arranged in rows and columns, filling the entire frame. Some bins have the 'Telesis' logo printed on them, while others have a small white label with a yellow square and the word 'Stack'. In the center of the grid, there is a large white rectangular area containing bold black text. The bins are shown from a slightly elevated perspective, showing their top and front faces. The overall composition is repetitive and emphasizes the quantity and variety of the storage solutions offered by Telesis.

**LAST YEAR TELESIS
SHIPPED 40% OF ALL THE
INTELLIGENT PCB/CAD
WORKSTATIONS IN THE U.S.**



THIS YEAR WE'VE GOT OUR DESIGNS ON CAE.

Our Telesis EDA-300 is simply the best PCB/CAD workstation in the industry.

That's because it thinks like a designer.

It handles just about any board technologies you can throw at it. Digital, analog, surface mount, hybrid, ECL and more.

And virtually any size board or density.

Our powerful automatic placement and 32-bit routing capabilities are exceptionally fast and fully re-entrant for easy editing.

All of which explains why Telesis has the largest installed customer base of intelligent PCB/CAD workstations in the U.S.

But that's just the beginning.

Because now Telesis is the first company to apply a systems orientation to Computer-Aided Engineering.

Our new Design Capture software runs on the low-cost IBM Personal Computer family. Since our software is fully integrated with the EDA-300 you can capture your schematics and forward net lists to PCB/CAD. As well as automatically back annotate and update the schematic.

You may transfer the details of your design directly to Teradyne's LASAR™ simulation software, which runs on our 32-bit Co-processor with the IBM PC. LASAR allows you to verify system designs with advanced features like true worst-case timing analysis and the most extensive model library available. Using LASAR for both design and test can typically save months in time.

Then with our unique Thermal Analyzer you can pinpoint hot spots on your board in just minutes. So board layout and packaging can be designed for optimum heat dissipation, leading to increased system reliability.

In short, no other CAE system can help you get your PCB product to market faster than Telesis.

Like to know more about our integrated products? Call (617) 256-2300. Or write

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Chelmsford, MA 01824.

Once you do, you'll have your designs on us.



*Dataquest Inc., based on total numbers of Standalone Workstations shipped in U.S. 1984.

™Teradyne

Telesis

CIRCLE NO 15

Introducing the HP 54100A/D 1GHz General Purpose Digitizing Oscilloscope. Now see waveforms you've

The waveform you see displayed here was captured by the new HP 54100A/D 1 GHz Digitizing Oscilloscope. It shows an unstable clock (top trace) and the resulting data at the Q output of a D flip-flop. Plus, it automatically positions the event of interest in the center of the display and shows the events in negative time that led up to the trigger. The new HP 54100A/D can easily capture rare events like this and hold them for you to analyze with no blooming or fading. What's more, you get this with 10 psec resolution and 1 GHz bandwidth necessary to capture subnanosecond transitions in today's high speed logic designs. And it does all this at the touch of a button.

The first truly general-purpose digitizing scope for dc to ECL.

With logic speeds pushing faster all the time, you need a scope that can deliver reliable measurement

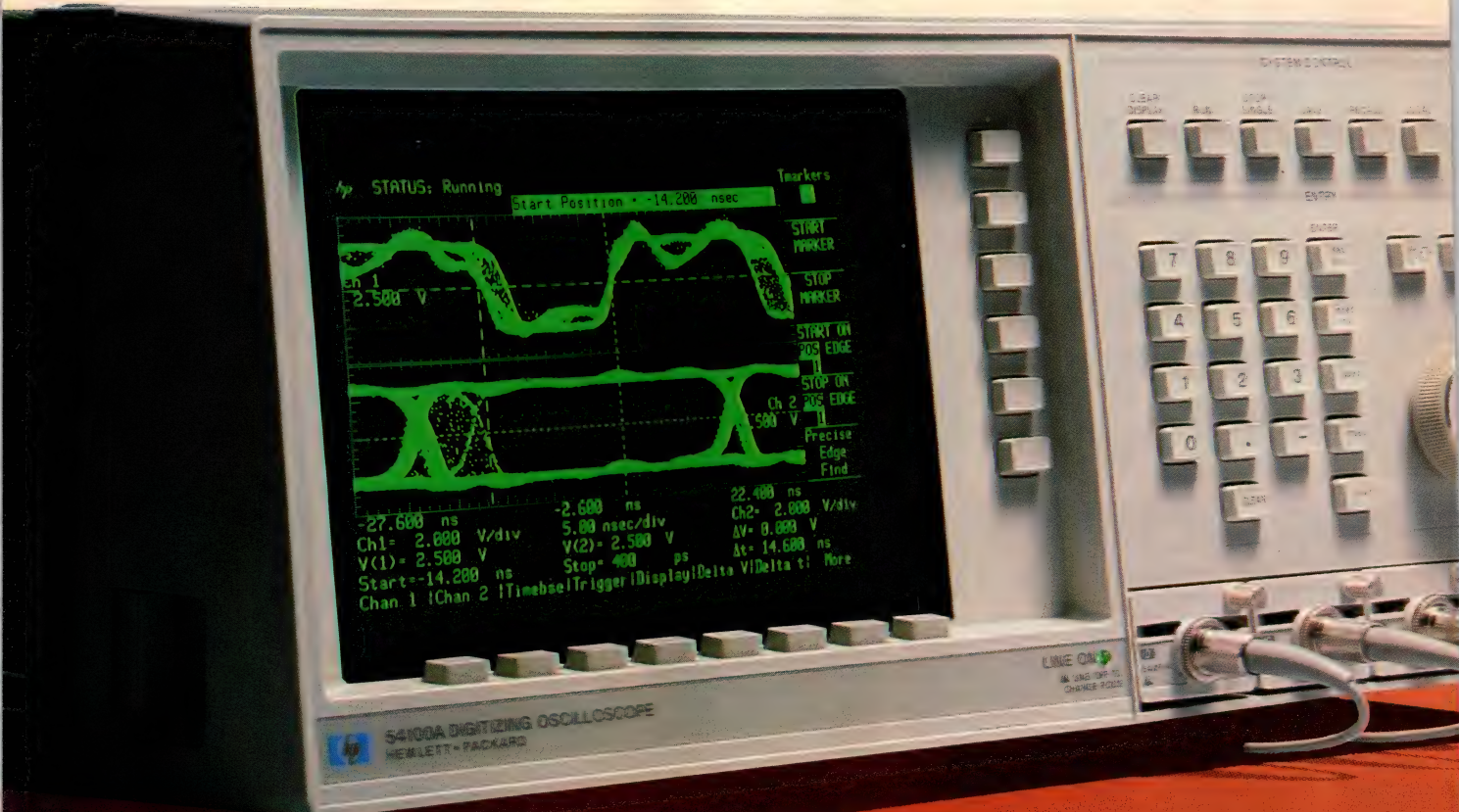
results from dc all the way to ECL. The new HP 54100A/D 1 GHz Digitizing Oscilloscope gives you that versatility. It combines a fast 350 psec rise time with a crystal-controlled timebase, sophisticated on-board analysis firmware, and easily re-configured inputs. It lets you see low duty-cycle signals with clarity and brightness not previously possible. You can even take it out of the lab into production. Make it a vital part of your computer-based ATE test system for even greater productivity and usefulness through HP-IB.

Complete one-button characterization of your high-speed waveforms.

With the HP 54100A/D Digitizing Oscilloscope, you can be productive as soon as you sit down in front of it. Simple keystroke sequences give you automatic pulse parameter measurements, automatic signal scaling and instrument setup, automatic hardcopy output (over HP-IB) and more. You can trigger on logic patterns,



HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.



never seen before.



time-qualified patterns or state, or you can delay the trigger by edge count or absolute time. The HP 54100A/D unloads much of the setup and test burden

from you so you can devote your time to designing.

Expanded probing capability and convenience.

Designed as a companion product to the HP 54100A/D, the new HP 54300A Dual 8:1 Probe Multiplexer expands your scope's two inputs to a total of 16. Use it as a front-end interface for your production ATE test system or as a bench test system for design characterization in your R&D lab.

High frequency, high impedance probing.

Whether you're in R&D or production engineering, you know the need for better, more flexible probing schemes. With the HP 54100A/D or the HP 54300A Probe Multiplexer, you can choose from 1 GHz minia-

ture probes, 50 ohm BNC inputs, or high-impedance 1 Mohm/300 MHz probes. Automatically setup and recall up to 100 test sequences of up to 99 steps each (3700 steps maximum), either from the front panel or under HP-IB control.

Call HP today. 1-800-835-5577.

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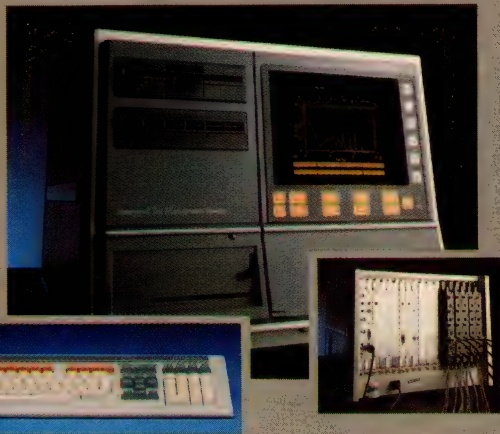
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NEWS BREAKS

EDITED BY JOAN MORROW

LOW-COST 32-BIT SUPERMICRO MATCHES MINICOMPUTER POWER

Based on the MicroVAX 78032 μ P, Digital Equipment Corp's (Maynard, MA) MicroVAX II supermicrocomputers and VAXstation II workstations deliver performance levels comparable to those of the company's VAX-11/780. Although you can't form VAX clusters with the new systems, you can link as many as 16 MicroVAX IIs in a LAN. All systems operate under VMS and Ultrix, DEC's implementation of Unix.

The company also released field-upgrade kits for the MicroVAX I microcomputer, as well as compact optical disks, each of which can store as many as 200,000 single-spaced typewritten pages. The single-user MicroVAX II system is available now; other systems will begin shipping in July. Prices for the MicroVAX II range from \$18,840 to \$43,780; the basic VAXstation II starts at \$26,500.—Eva Freeman

RAM-DISK SUBSYSTEM INCLUDES FAIL-SAFE FEATURE

The Model 7900 semiconductor disk subsystem (SCD) from National Advanced Systems (Mountain View, CA, (415) 962-6000) will combine the data-access speed and capacity of a RAM disk with a built-in hard-disk device for emergency storage. In the event of a power loss to the RAM disk, the hard disk will record all the data stored on the SCD. The SCD, which is scheduled for release in August, will consist of a control unit, as many as four semiconductor memory units, and a battery backup unit with a built-in magnetic disk.

Each memory unit will be available in 32M-byte increments for a maximum of 128M bytes per unit, or 512M bytes per SCD. The memory units will also feature dual ports that provide the system with an aggregate 6M-byte/sec data-transfer rate. A typical configuration with 128M bytes of memory will cost \$498,800.—J D Mosley

TEKTRONIX OFFERS CUSTOM AND SEMICUSTOM SERVICES

Tektronix (Beaverton, OR) has opened its Integrated Circuits Operation to outside customers by offering semicustom linear arrays and custom foundry services. Both the semicustom and custom ICs will feature high-bandwidth bipolar transistors ($f_T = 6.5$ GHz), laser-trimmable resistors, and fast turnaround—three weeks to fabricate a Quickchip from layout and eight weeks to fabricate a full custom IC, which is roughly one-half the industry average.—David Smith

NORTHEASTERN UNIVERSITY OPENS TECH CENTERS IN CALIFORNIA

Northeastern University (Boston, MA) has announced plans to open six regional technology centers in Silicon Valley this September. Nearly 100 specialized high-technology courses will be offered in a continuing-education program for professional engineers, scientists, and managers. Northeastern will pattern its Bay Area Regional Technology Centers (Santa Clara, CA, (408) 986-8480) after its continuing-education programs in the Boston area, which started in 1963.

To accommodate the rapidly changing nature of high technology, courses will be taught by working engineers who deal with state-of-the-art devices and processes. Topics will range from IC fabrication to software management and development. The centers will schedule courses to suit working engineers' timetables.—Denny Cormier

NEWS BREAKS

INDUSTRY LEADERS REVIEW DISK HEAD/MEDIA TECHNOLOGY

On July 14, industry leaders will meet in Chicago to discuss such issues as media corrosion; static and dynamic friction; whether overcoating of media is necessary; and the special problems related to sub-4-in. disk heads. The review, which will coincide with NCC/85, is sponsored by Peripheral Research Corp ((805) 963-8081) and Don Mann Magnetics Inc ((805) 496-2999). Speakers from Ampex, Applied Magnetics, Brown Disk, Cyberdisk, Information Magnetics, Read-Rite, and 3M will participate.—Ed Teja

TWO SUPERMINICOMPUTERS TARGET ENGINEERING AND CAD

Harris Computers' (Fort Lauderdale, FL) 7-MIPS HCX-7 and 5-MIPS H1200 superminicomputers are designed for scientific and engineering applications. Operating under a native AT&T Unix V system, the HCX-7 is the first 32-bit computer developed by the vendor. By using a reduced instruction set (160 instructions), the HCX-7 can implement most instructions in one 100-nsec machine cycle. Prices for the HCX-7 begin at \$225,000; shipments start in July.

The H1200 boosts its performance by incorporating ECL memories and by implementing many scientific and mathematical functions in hardware. Designed around an 80M-byte/sec ECL bus structure, the memory units feature either 270- or 135-nsec cycle times. The H1200 starts at \$294,000, and shipments will begin in September.—Eva Freeman

ALL-ELECTRONIC UNIVERSITY SIGNS FIRST COMPANY-WIDE SPONSOR

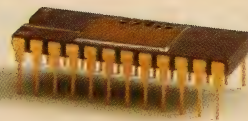
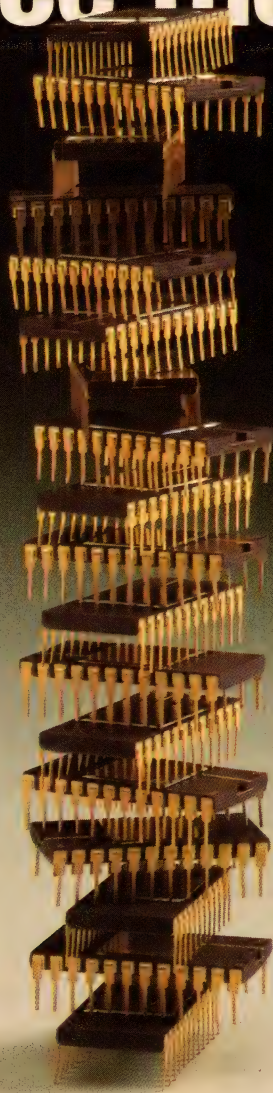
Hewlett-Packard Co (Palo Alto, CA) recently became the first National Technological University (NTU) corporate client to take out a company-wide subscription. Based in Fort Collins, CO, NTU is an all-electronic university offering videotaped graduate-level engineering courses to companies enrolled as corporate clients. Among its corporate subscribers are Digital Equipment Corp, IBM, Eastman-Kodak, and Motorola. Typically, corporate subscribers pay a fee for each company facility that accesses the videotaped courses. Hewlett-Packard is the first client to open up the use of NTU to employees at all of its facilities.

NTU offers masters-degree programs in computer engineering, electrical engineering, and engineering management. All of its courses are available on videotape. This fall, however, the school expects to begin broadcasting its classes via satellite.—Deborah Asbrand

GRAPHICS SOFTWARE PACKAGE IMPLEMENTS ANSI AND ISO LEVEL 2B

The GSS-Toolkit Kernel System is a linkable library of graphics routines that lets you write programs in C, Fortran, or Basic and use one set of interfaces to the graphics routines. An implementation of the ANSI and ISO specification level 2b, the package from Graphic Software Systems (Wilsonville, OR) is available to OEMs using MS-DOS, PC-DOS, Unix System III, V, or 7, or Unix Berkeley 4.2. Versions for other operating systems are available on a custom basis.—Ed Teja

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Why fill your digital delay design with unnecessary components, when you can have all the capability you need in one small, low-cost IC?

TRW LSI Products Division, the industry leader in high performance digital signal processing products, gives designers an edge with the TDC1011. The TDC1011 is a high-speed, 8-bit wide shift register, programmable to any length between 3 and 18 stages. It operates at an 18MHz shift rate (56ns worst case), is TTL compatible, and dissipates a low 750mW.* The TDC1011 operates from a single +5V power supply and is available in a 24-lead DIP.

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NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

UNIX SUPERMICRO EMPLOYS THREE SEPARATE PROCESSORS

The Unix-based multiuser Mentor supermicrocomputer from Integrated Micro Products (Consett, UK, TLX 53429) incorporates three separate VME Bus processor cards. The ET-68020 CPU card features a 16-MHz 68020 μ P and a memory-management unit, which is implemented using TTL logic and static RAM to provide high-speed address translation. Local processor memory resides on as many as four memory cards, each holding 2M bytes of 32-bit memory. The memory cards reside in VME card slots adjacent to the CPU and are accessed via a dedicated high-speed memory bus.

For processor-intensive tasks, the CPU and memory system execute benchmarks three times faster than a VAX 780. The CT-68VIDC intelligent disk controller and CT-68VICP intelligent communication controller each incorporate an onboard 68000 processor. The CT-68VIDC features a disk cache buffer of 512k bytes max of dual-ported RAM and an SCSI bus to support multiple drives. The communication controller has 128k bytes of onboard RAM and supports 16 asynchronous serial ports, two synchronous serial lines, and 48-bit parallel I/O. Prices for the Mentor system start at approximately £15,000.

PASCAL COMPILERS ARE VALIDATED TO CLASS A STANDARDS

The 3L range of Pascal compilers from Lattice Logic (Edinburgh, UK, TLX 72465, Attn Lattice) includes versions for the DEC VAX running under VMS and Unix, the Perkin-Elmer 3200 running under OS32 and Unix, the Whitechapel MG-1 running under Genix, and the Acorn NS32016 second processor running under Panos. The compilers, written to port the company's CAE software onto a variety of CAE workstations, are all class A validated to the Pascal standard BSI-6192 Level 1 (ISO) 7185. Versions are currently under development for Apollo Domain and Sun workstations and IBM 370-type machines. Prices range from £1000 to £6000 depending on machine.

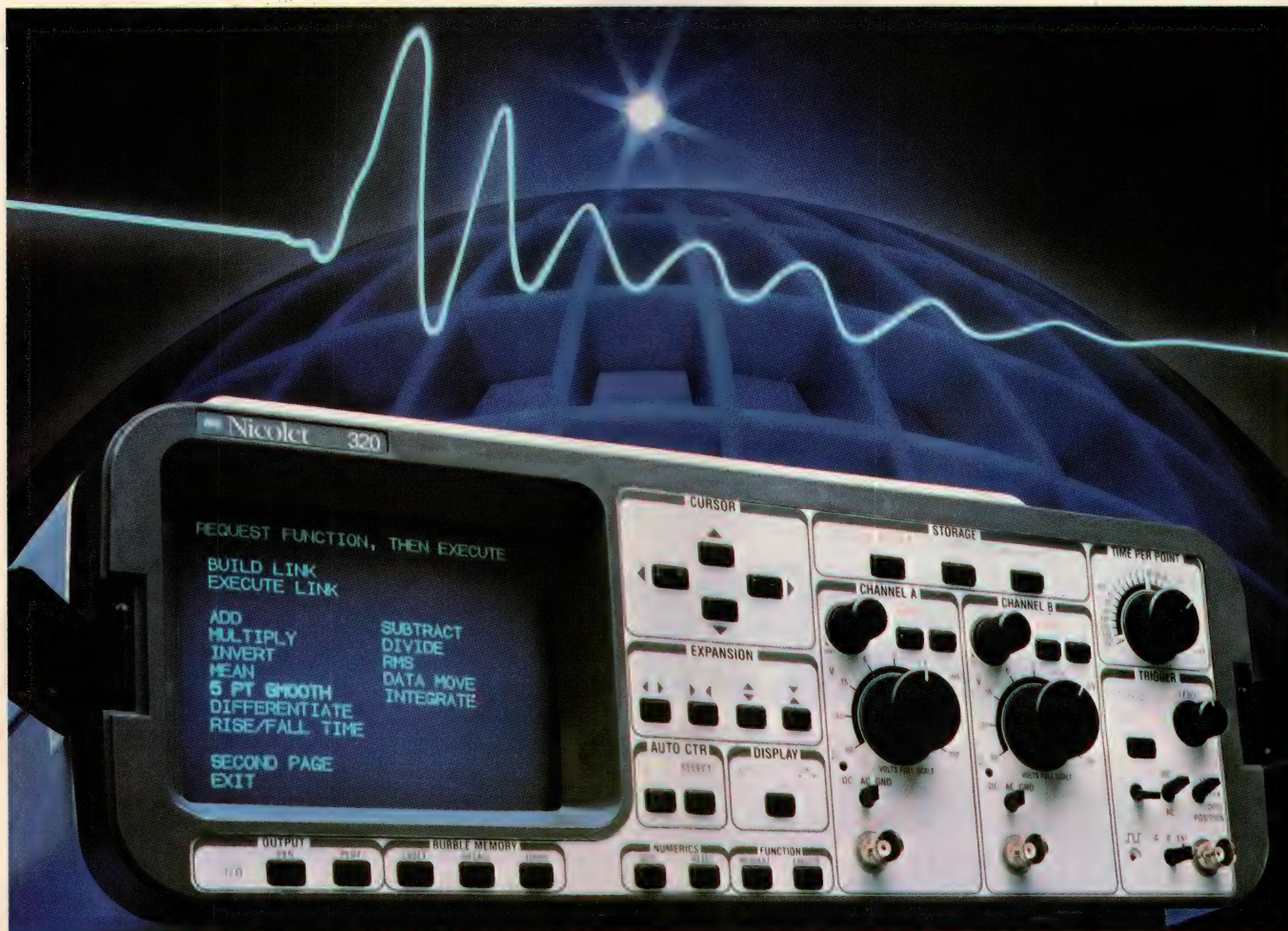
COLOR CRT CONTROLLER MANIPULATES 16 IMAGES

The 82716 video-display controller, separately manufactured by Matra-Harris Semiconductors (Nantes, France, TLX 711930) and Intel Corp (Santa Clara, CA), allows you to define as many as 16 variable-sized, colored object images, and to move them around in or out of a video frame. Object images can be bit-mapped graphics or alphanumeric characters, and you can program them to have prioritized overlap and transparency attributes. Maximum screen resolution is 640 x 512 pixels with four bits/pixel, allowing you to select 16 colors from a palette of 4096 in an on-chip color look-up RAM. The 82716 is NAPLPS and CEPT compatible. Silicon is currently being run by Matra-Harris; the company expects the device to have a sample price of around \$80 and a target volume price of \$20.

PATTERN GENERATORS SERVE ALL MAJOR TV STANDARDS

Philips Test & Measurement Div's (Eindhoven, The Netherlands, TLX 35000) PM-5515, -5516, and -5518 TV test-pattern generators are adaptable to PAL, NTSC, and SECAM standards. The instruments cover IF and VHF bands I and III, S-band cable channels S1 to S20, and UHF bands IV and V. Versions are available for testing Teletext/Antiope, and PAL stereo FM receivers. Options include RGB outputs.

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Manipulate stored waveforms via a menu of mathematical routines using only two buttons. Set-up fully automatic sequences for unattended operation. Store up to four 4,000 point waveforms and examine in detail using digital expansion and the annotated display.

Communicate data via the built-in GPIB and RS232 interfaces. Output for hardcopy to XY or YT recorders or digital plotters.

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The 320 is so easy to use the manual is almost superfluous. Easy to carry too. The lightweight package includes storage for probes, power cable and, just in case, the manual.

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For more information call toll free 1-800-356-3090 (Wisconsin: 608/273-5008). In Canada, call 416/625-8302. Or write: Nicolet Oscilloscope Division, 5225 Verona Rd. Madison, WI 53711.

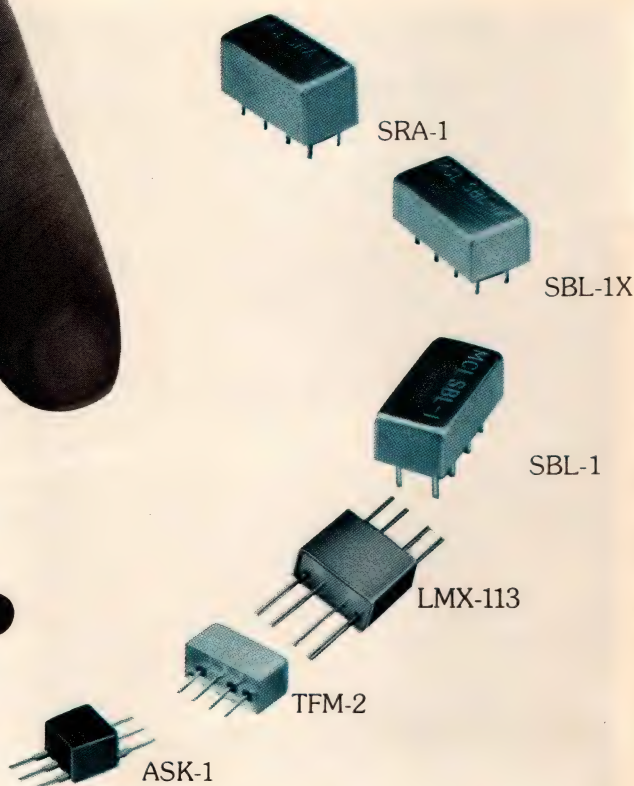


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SBL-1	world's lowest cost industrial mixer, only \$4.50, metal case	1-500	DC-500	5.5 typ.	6.5 typ.	50 typ.	45 typ.	35 typ.	3.95 (100) 4.50 (10-49)
SBL-1X	industrial grade, rugged all-metal construction	10-1000	5-500	6.0 typ.	7.0 typ.	50 typ.	40 typ.	30 typ.	5.95 (10-49)
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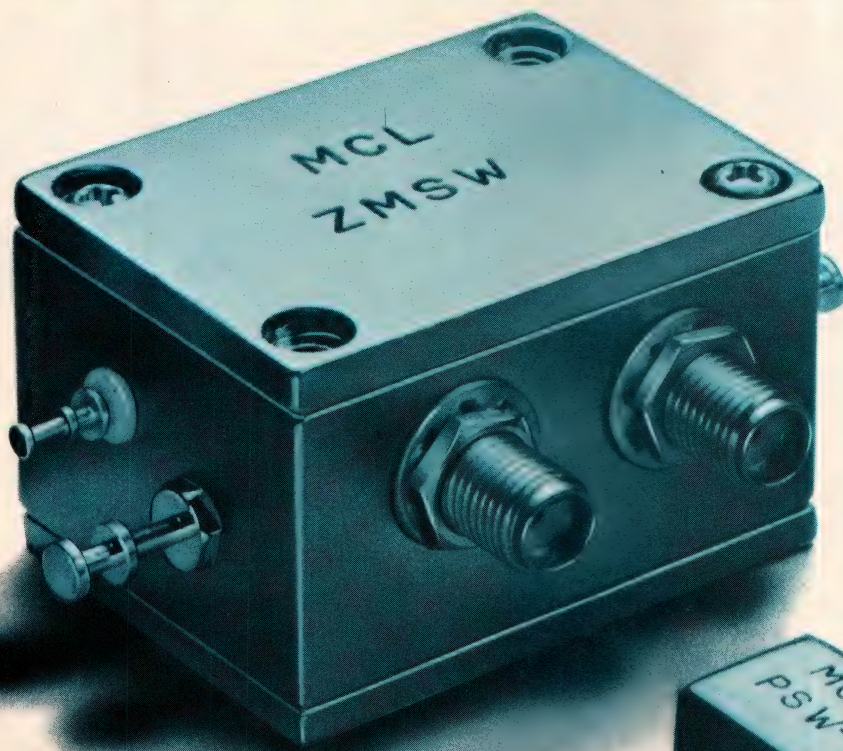
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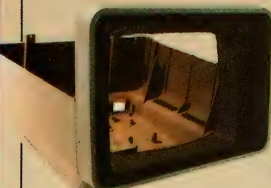


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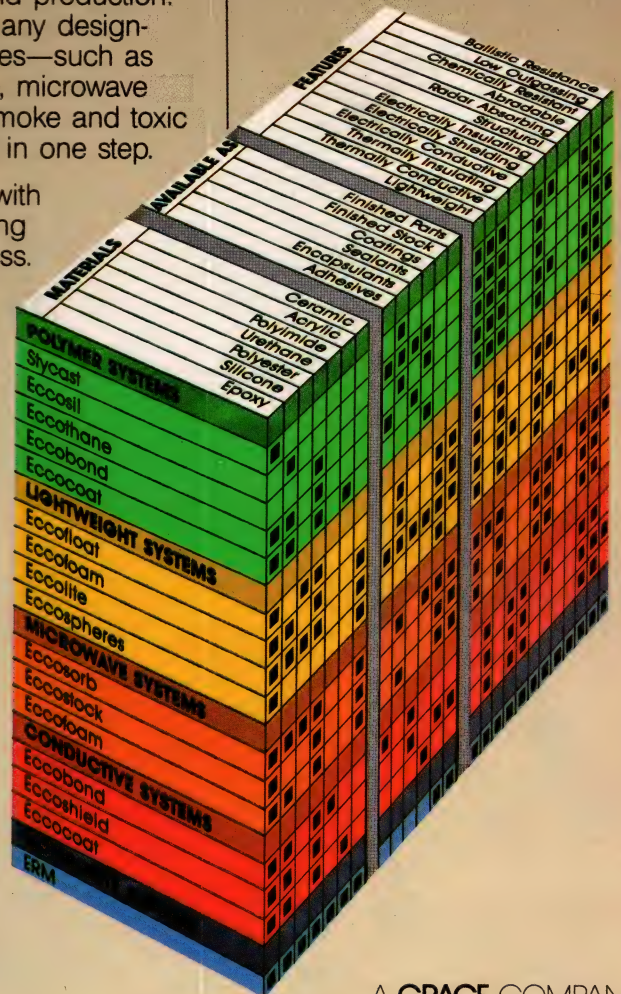


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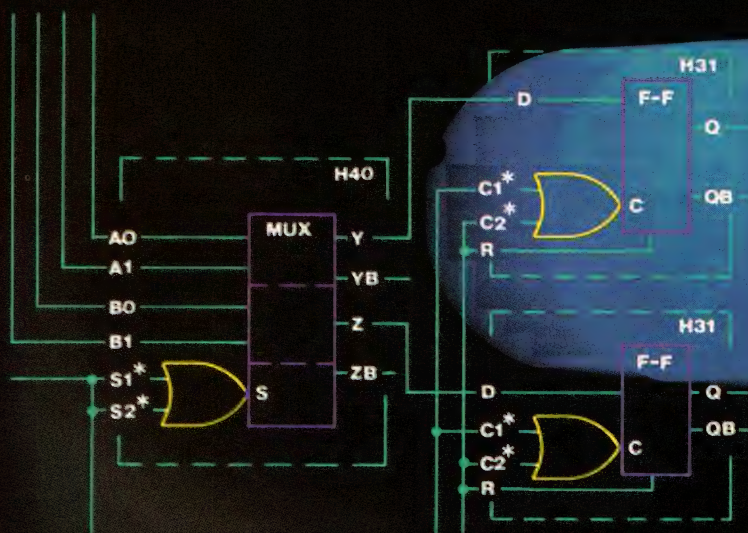
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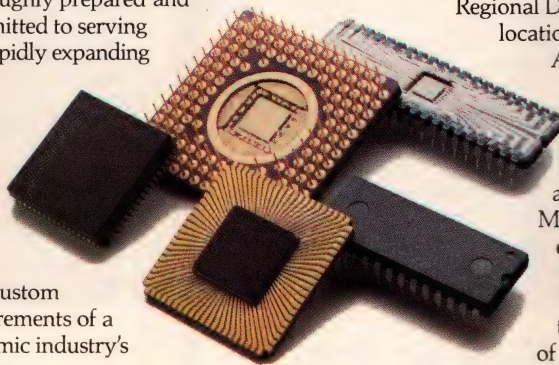
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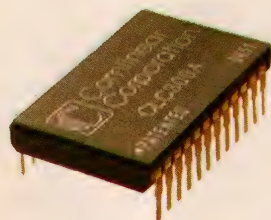
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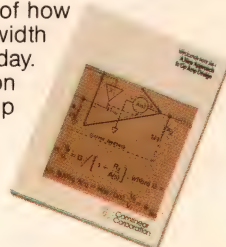
At Comlinear, we'd like to clear the air with some straight talk on gain/bandwidth products. Our CLC300 op amp delivers a fixed -3dB bandwidth of 85MHz. No more gain/bandwidth product. To do that, we've had to rewrite the book on op amp design and gain/bandwidth relationships. In fact, unlike most op amps, all key specs remain unchanged across a wide range of gains. Now you have an op amp that delivers the performance you need under real circuit conditions. And if that's not good enough, try this: the CLC300 is available for only \$39* in 100-piece quantities.

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CIRCLE NO 22

SIGNALS & NOISE

Misleading statements about digital encoders

Dear Editor:

"Sensor, ADC specs set angular-measurement system's performance" (EDN, January 24, pg 165) by Geoff Boyes of Analog Devices contained some statements which I believe to be misleading.

The statement I object to most appears in the top right-hand column on pg 166, where Mr Boyes states: "Although absolute encoders overcome the problem of absolute-position certainty at power-up, transmitting those encoders' parallel digital outputs through noisy environments is far from easy. Long distances necessitate the addition of line drivers, repeaters, or both; moreover, wide digital words drive up wiring costs."

In current engineering practice, which is easier, transmitting analog signals over long distances, or transmitting digital signals over long distances? The main basis of acceptance of digital telephony or pulse-code modulation has been that once a signal is digitized, it can be transmitted in virtually an error-free state. When noise is added to an analog signal within the passband of the signal, it can never be removed. The portion of the state-

ment relative to noise in Mr Boyes's article is nonsense.

Mr Boyes's remarks also contained a misstatement about wiring complexity. Modern encoders with either serial or data-bus output formats can interface the encoder with as few as five wires. Note that in Fig 2 of the article, six wires are shown between the resolver and the converter. Ittek has discovered through its experience in dealing with customers in the aerospace industry that most high-accuracy resolvers using compensation windings require 10 to 12 wire interfaces.

Sincerely,

Donald H Breslow

Director of Engineering
Ittek Measurement Systems
Newton, MA

Author's response

Dear Editor:

Mr Breslow is, of course, quite correct to state that once noise is added to an analog signal within its passband, it can never be removed. The same is also true of digital signals, unless some form of error correction is incorporated. The key point here is to consider the effective passband of a resolver-to-digital converter.

The output signal from a resolver consists of amplitude information modulated onto an ac carrier waveform. To decode all this, modern tracking converters of the type described in my article include a phase-sensitive demodulator that will respond only to signals that are phase and frequency coherent with the known carrier signal. When you combine the phase-sensitive demodulator with the second-order lowpass-filter characteristic inherent in any type II tracking converter, the result is an effective noise passband that is a narrow slot (typically a few hundred hertz wide) in the frequency spectrum.

To assert that the transmission of digital data is inherently more secure than the transmission of analog data, irrespective of the technique employed, is fatuous. The noise-rejection performance of digital-data-transmission systems that include comprehensive signal conditioning and error detection (LANs and modems are good examples) can be very high indeed. Similarly, the ability of a resolver-to-digital converter to reject, for example, noise breakthrough from a PWM motor drive (often found alongside angle transducers) can be demonstrated to be excellent. However, to attempt to transmit unconditioned TTL signals over any significant distance, relying on no more than a few hundred millivolts of hysteresis in standard line receivers, is clearly asking for trouble. This is the point I was making: With a resolver and converter, the data-transmission system is built in. With most optical encoders that are available, users must add the data-transmission system themselves.

Regarding the number of interconnections necessary for various angle-measurement transducers, resolvers need only six wires. The compensated devices to which Mr Breslow refers are intended for trigonometric computing applications and not for simple angle measurement. The comment I made about interconnect costs for encoders was aimed at true absolute encoders that output parallel data. Given that resolver-to-digital converters have resolutions of 10 to 16 bits, a comparable absolute encoder must always have more interconnections. Incremental encoders can certainly have fewer output connections, but these devices have other problems, as I pointed out in the article.

Sincerely,

Geoff Boyes

Analog Devices Ltd/
Memory Devices Ltd
East Molesey, Surrey, England



SIGNALS & NOISE

Using digitizing oscilloscopes

Dear Editor:

I enjoyed the Special Report on digitizing instruments (EDN, March 7, pg 112), and I recommend it to anyone who works with automatic test equipment.

I would like to stress that perhaps the most difficult aspect of using a digitizing oscilloscope is the development of efficient algorithms for analysis of the data that represents the digitized waveform.

One is seldom so fortunate as to simply have to determine frequency or pulse width, especially since an electronic counter can measure such parameters directly. Usually, you must determine whether a noisy, jittery waveform has a certain amount of overshoot, ringing, droop, or rise time, or a complex form. An operator can determine such characteristics by observation,

but an automated system must analyze a large number of data points in a way that gives the correct answer within a reasonable time. Coming up with straightforward and accurate techniques to do the job can present a formidable challenge to any engineer.

Sincerely,
Allan C Stover
Ellicott City, MD

Analog input bandwidth is important for digitizing tools

Dear Editor:

The Special Report on digitizing instruments by Charles H Small (EDN, March 7, pg 112) was well done and very comprehensive. Especially interesting was the editorial box on pg 116 and 117. One could consider this to be a *Consumer Re-*

ports-style selection guide.

Having worked at Biomation (now Gould Santa Clara) in marketing/applications in the early days of transient recorders (Biomation was a pioneer in the field), I wish to discuss a few points that Mr Small brought out in the box.

First, it is true that, for capturing transient events, the most important spec is digitizing rate. However, the analog input bandwidth is another important consideration.

When you look at transients in the frequency domain, you find that they're wideband signals. The input bandwidth is little more than an indication of how the transient pulse will be softened. On the other hand, the most important aspect of the input bandwidth is how close it is to the maximum sample rate.

The analog bandwidth should be $\frac{1}{3}$ to $\frac{1}{4}$ of the sampling frequency, because this tends to minimize ali-

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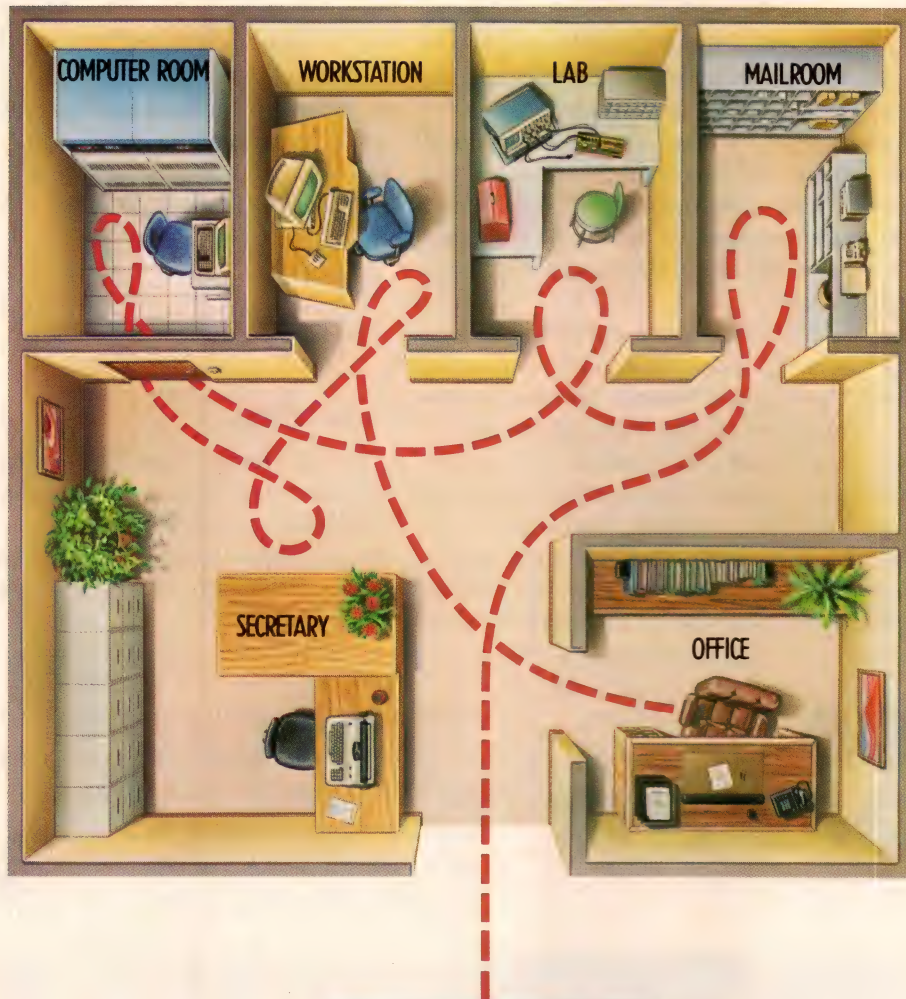
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asing, which is a source of inaccuracy in measurement. Input bandwidth closer to the sample rate is permissible only if the input filter in the analog stages before the A/D converter has a very sharp cutoff.

The desire for more bits of resolution in the A/D converter is often a result of the user's desire to have a wide dynamic range, because a 10-bit A/D converter has a dynamic range (1 in 1024) that's four times that of an 8-bit unit (1 in 256). Many transients are only generally characterized before they're captured and examined, so it pays to be able to capture more information in one shot—and a 10-bit A/D converter captures more information.

Mr Small also discussed the dead time between one capture cycle and the time the instrument is ready to capture again. There are two probable reasons why manufacturers didn't supply this information; they

have never measured it, or they realized that the time is completely dependent on how fast the mass-storage device can accept the data. This was always the limiting factor with Biomation instruments; the unit could dump faster than contemporary minicomputers could take it, even under DMA operations.

As a stickler for detail, I must point out that Mr Small used the terms "accuracy" and "resolution" interchangeably under the section entitled "Accuracy specs are inaccurate."

Accuracy is the condition of conformity to a model; in the context of the engineer's world, the models are provided by the National Bureau of Standards and relate to how closely an instrument can indicate the true value of a physical quantity.

In the context of A/D converters, resolution is an expression of how many discrete levels there are be-

tween the instrument's plus and minus full-scale input range; resolution has nothing to do, per se, with accuracy as defined above. Effective resolution is, as Mr Small implied, an expression of how the A/D converter reacts to high dV/dt signals.

In sum, the article was great, and it points up the current high interest in instruments of this type.

*Sincerely,
Edward S Jacklitch
San Jose, CA*

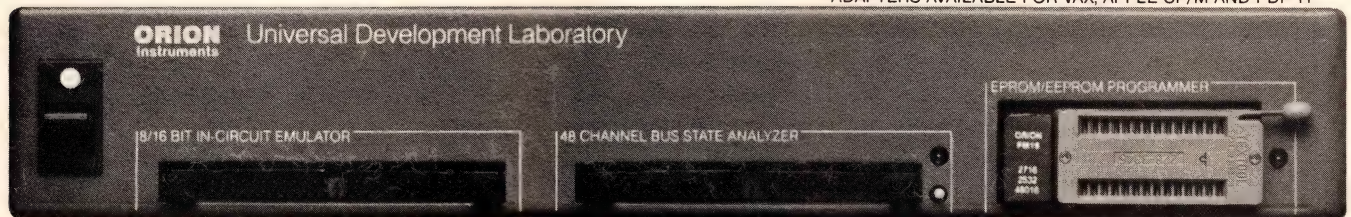
Correction

In the Design Idea "Programmable calculator solves congruence," by Shlomo Varsano (EDN, December 13, 1984, pg 368), line 13 of the program should read "ST*Y", not "STO Y".

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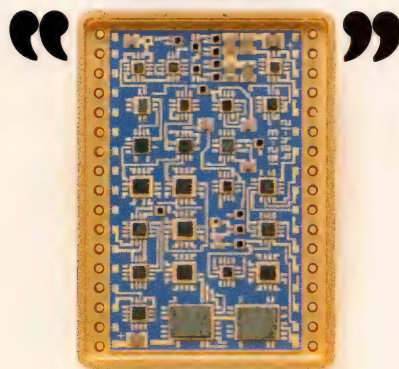
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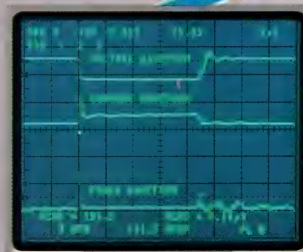
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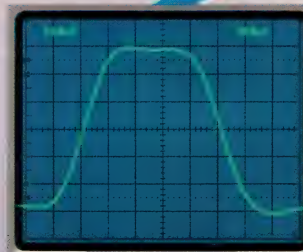
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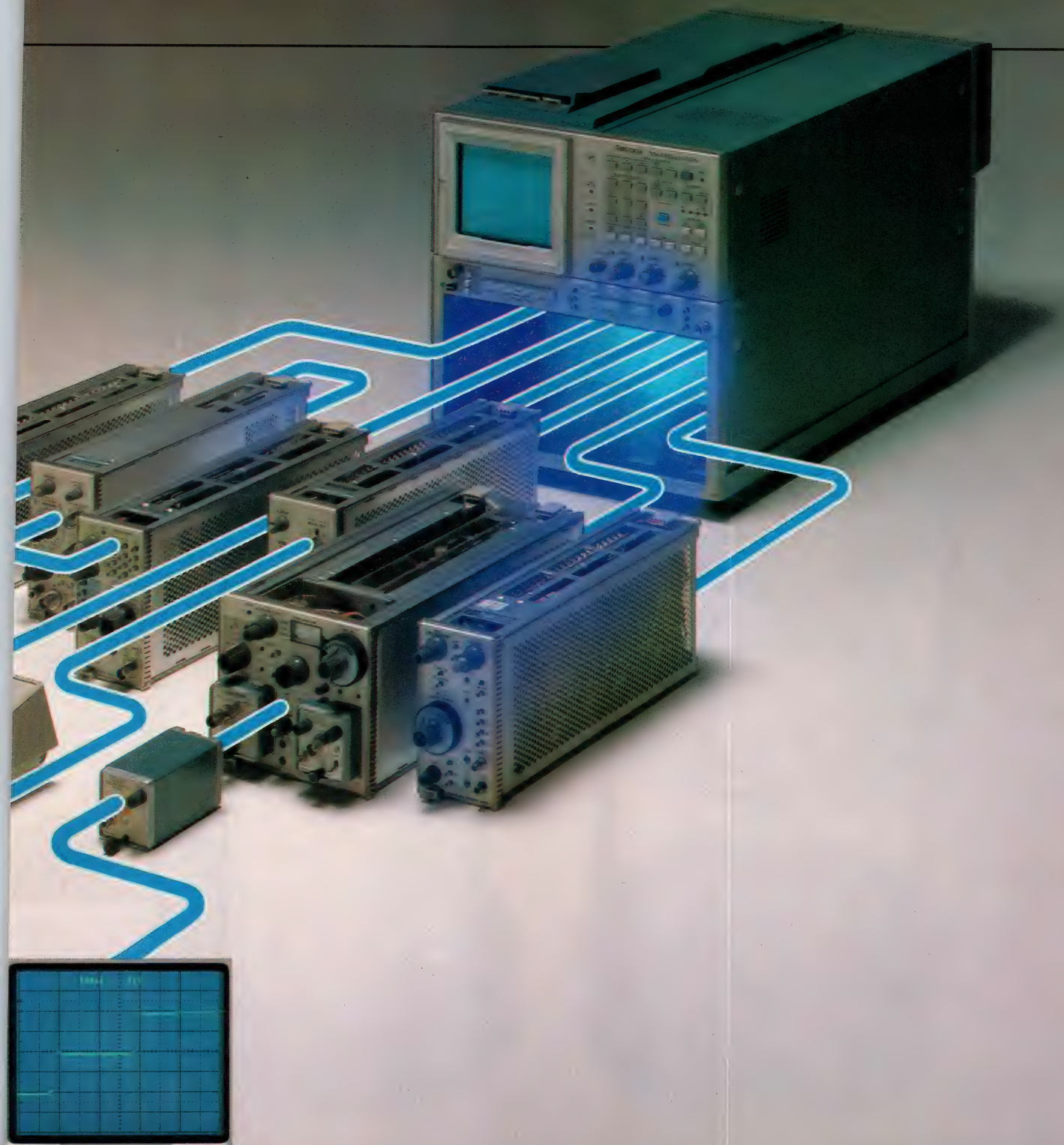
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Fiber Optics to the Year 2000, Monterey Conference Center, Monterey, CA. Eloise Beckett, Electronicast Corp, 40 Birch St, Redwood City, CA 94062. (415) 365-1322. June 17 to 18.

Nepcon East, Bayside Exposition Center, Boston, MA. CEG, Box 5060, Des Plaines, IL 60018. (312) 299-9311. June 19 to 21.

Society of Women Engineers National Convention, Minneapolis, MN. SWE, 345 E 47th St, New York, NY 10087. Phone (212) 705-7855. June 23 to 30.

International Electronic Printer Industry Conference, Brussels, Belgium. CA Pesko Associates Inc, 1 Snow Rd, Marshfield, MA 02050. (617) 837-1341. June 24 to 26.

Programming in C: A Hands-on Workshop, Boston, MA. Ruth Dordick, Integrated Computer Systems, Box 45405, Los Angeles, CA 90045. (800) 421-8166; in CA, (800) 352-8251. June 25 to 28.

Semicon/Osaka '85, Osaka, Japan. William Galarneau, SEMI, 625 Ellis St, Suite 212, Mountain View, CA 94043. (415) 964-5111. June 25 to 26.

Management Skills for New and Prospective Managers (seminar), New York, NY. New York University, School of Continuing Education, 575 Madison Ave, New York, NY 10022. (212) 580-5200. June 26 to 28.

Legal Issues in Acquiring and Using Computers (seminar), New York, NY. New York University, School of Continuing Education, 575 Madison Ave, New York, NY 10022. (212) 580-5200. June 27 to 28.

Writing Better User Manuals, Denver, CO. Battelle Memorial Institute, 4000 NE 41st St, Seattle, WA 98105. (800) 426-6762; in WA, (206) 527-0542. June 27 to 28.

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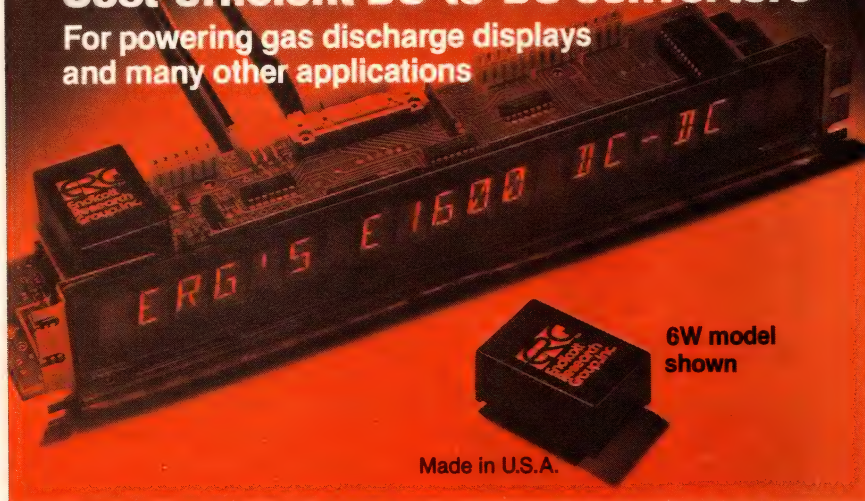
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CADMAT-Asia '85 (Computer-Aided Design, Manufacture, and Test), Mandarin Hotel, Singapore. Bryman-Bull Ltd, 1716 Monticello Rd, San Mateo, CA 94402. (415) 345-3603. July 9 to 11.

How to be Effective as a Technical Manager, Washington, DC. Ruth Dordick, Integrated Computer Systems, Box 45405, Los Angeles, CA 90045. (800) 421-8166; in CA, (800) 352-8251. July 9 to 12.

Principles of Microcomputers and Microprocessors (short course), Ann Arbor, MI. University of Michigan, Continuing Engineering Education, 300 Chrysler Center/North Campus, Ann Arbor, MI 48109. (313) 764-8490. July 15 to 19.

Programming in C: A Hands-on Workshop, Los Angeles, CA. Ruth Dordick, Integrated Computer Systems, Box 45405, Los Angeles, CA 90045. (800) 421-8166; in CA, (800) 352-8251. July 16 to 19.

Computer Simulation Conference and Exhibits, Westin Hotel, Chicago, IL. Charles Pratt, The Society for Computer Simulation, Box 2228, La Jolla, CA 92038. (619) 459-3888. July 22 to 26.

How to be Effective as a Technical Manager, San Diego, CA. Ruth Dordick, Integrated Computer Systems, Box 45405, Los Angeles, CA 90045. (800) 421-8166; in CA, (800) 352-8251. July 23 to 26.

1985 Microelectronics Interconnect Conference, Rippling River Conference Center, Welches, OR. International Society for Hybrid Microelectronics, Box 3255, Montgomery, AL 36109. July 29 to 31.

Programming in C: A Hands-on Workshop, Washington, DC. Ruth Dordick, Integrated Computer Systems, Box 45405, Los Angeles, CA 90045. (800) 421-8166; in CA, (800) 352-8251. July 30 to August 2.

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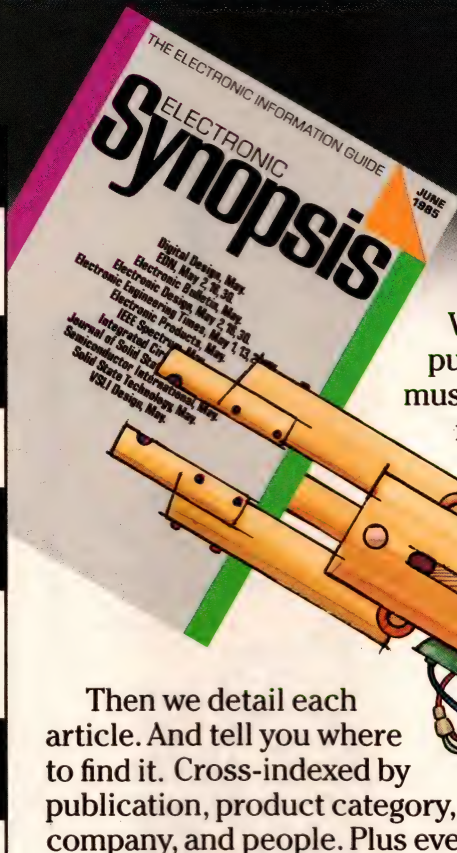
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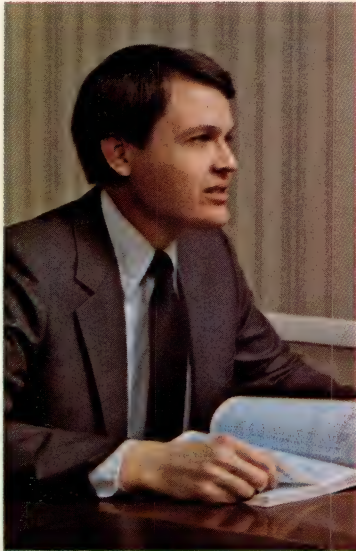
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CIRCLE NO 34

EDITORIAL

μ P history repeats itself



Barely a decade ago, microprocessors were new and largely unknown. Except for a small cadre of technology leaders, engineers were still evaluating the new devices and learning how to apply them. Then, in seemingly no time at all, μ Ps were everywhere—in such visible applications as personal computers and in countless invisible roles ranging from home appliances to industrial machinery. Now, only a decade later in time, but generations later in technology, 32-bit μ Ps are repeating some of the history written by their 4-, 8-, and 16-bit predecessors. And many of the lessons that we learned a decade ago are lessons that we must learn again today.

One of the most important lessons is that a new technology will eventually find uses that aren't immediately obvious. Just as the early μ Ps found uses beyond calculators and personal computers, so will the new 32-bit devices find applications beyond workstations and minicomputers. Like their predecessors, 32-bit devices will play numerous invisible roles in embedded systems—in robotics, for example, where rapid, real-time response and high precision are essential, or in machine-vision systems, where image processing requires high-speed, high-precision number crunching. And like 4-, 8-, and 16-bit embedded- μ P systems, 32-bit embedded systems will require special hardware and software development tools, a topic that we address in this issue's cover story.

If you're one of the relative few who are already designing 32-bit systems, you know that your choice of 32-bit development systems, like your choice of 32-bit μ Ps, is still limited. As associate editor Charles Small points out in his article, however, not all approaches to 32-bit-system development require traditional in-circuit emulation. Your options, depending on the type of application you're developing, can include ROM emulation or even software development directly on your target system. In the latter case, an off-the-shelf, ROM-resident, real-time operating-system kernel might allow you to begin developing application software immediately.

So the outlook today, in many ways, is much as it was a decade ago. New μ Ps can help you solve previously unsolvable problems and create entirely new applications, but choosing the right μ P is just as difficult as it was then, if not more so. In addition, learning how to apply 32-bit devices—devices that are at least an order of magnitude more complex than their immediate predecessors—is a challenge comparable to applying the first, revolutionary μ Ps. In this issue of EDN and in issues to come, we'll help you meet that challenge.

Gary Legg

Gary Legg
Editor

PS. Cahners Publishing Co has moved to a new location. You can now contact EDN magazine at 275 Washington St, Newton, MA 02158; phone (617) 964-3030.

The new HP engineering drawing system.

You may think you're looking It could pay you to look again.

Actually, you're looking at a new computer-aided drawing system. We call it the HP Engineering Graphics System or HP EGS. And fortunately, it fits right in between time-consuming drawing boards and full-blown CAD systems—which makes it very affordable.

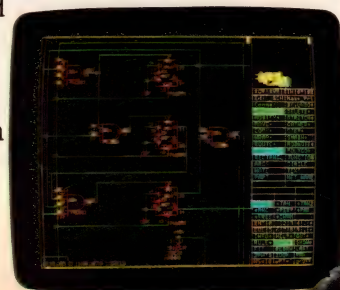
Whether you're involved in circuit or PC board design, mechanical engineering, technical writing or drafting, HP EGS can significantly reduce your manual drawing time and labor costs. And if you've been using a CAD system for technical drawing, HP EGS can eliminate waiting periods and free the CAD system for its more specialized tasks.

The right tools for schematics and PC board layouts.

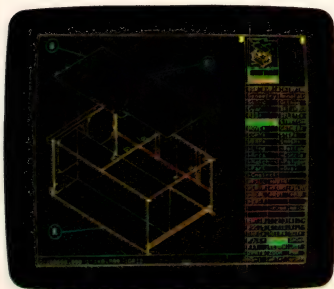
When preparing schematic drawings, HP EGS makes your task faster and easier. You'll have access to a sample library that contains over 50 already drawn components. And simple English commands allow you to create and save new parts.

When it comes to drawing PC board layouts, HP EGS offers more time-saving features. For example, a Rat's Nest Generator will automatically make all appropriate connections between PC board components. All components can be moved and traces rerouted while your connections remain intact. A step and repeat command saves time when your PC board design includes many ICs in a symmetrical pattern. And you save more time by using a sample library of over 40 PC board elements. Options, such as tooling outputs for photo-plotters and NC drills, are also available.

Once you've completed your schematic and PC board layouts, HP EGS will generate parts and connection lists. And there's a Connect List Compare



at a CAD system.



function to verify that your schematic and PC board connection lists are equivalent.

In addition to preparing PC board layouts and schematics, you can also use HP EGS to create other engineering artwork, such as detailed product and assembly drawings. And with an optional document editor, you'll be able to merge text and graphics for technical documentation.

A system you can tailor to your present and future needs.

Even if you have no prior programming experience, you can customize HP EGS to your exact needs. Customizing can include simple screen menu changes,

additions to the parts libraries, and the development of new drawing environments. And of course, you have a variety of Hewlett-Packard computers and peripherals to choose from.

Teamed up with our MC68000-based workstations, HP EGS offers networking capabilities that allow users to share data and peripherals. In addition, an optional IGES (Initial Graphics Exchange Specification) translator lets you transfer your drawings between HP EGS and CAD systems.

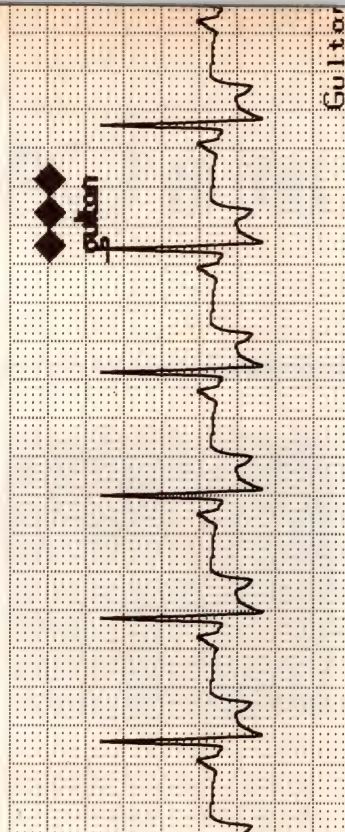
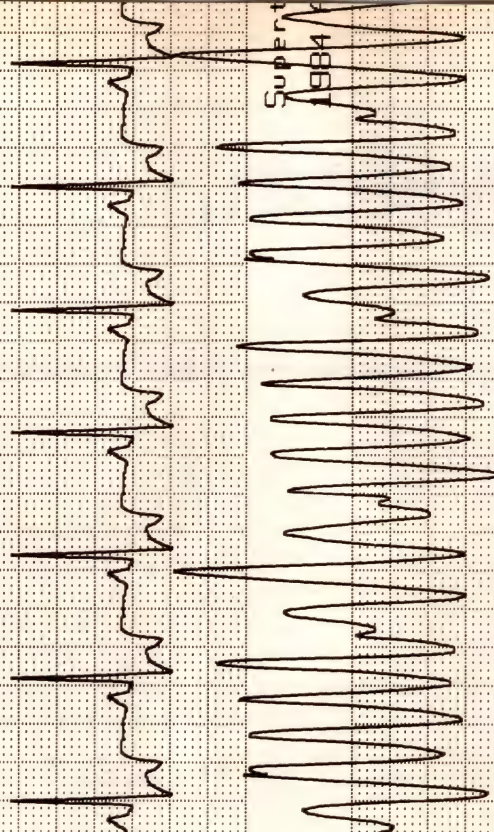
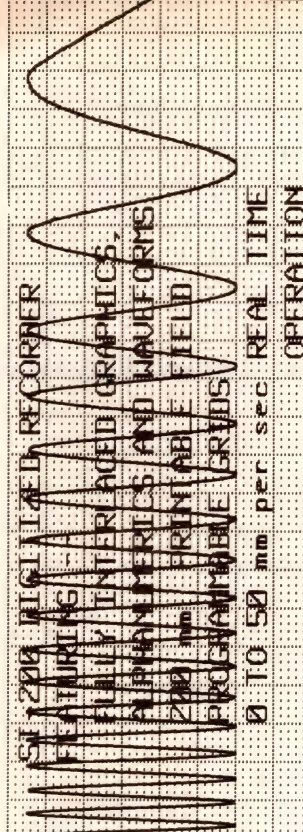
The advantages of choosing HP.

There's still more to HP EGS. You can also count on documentation, training, plus worldwide support and service. For complete information on HP EGS, call your local HP sales office. You'll find us listed in the telephone directory white pages.



**HEWLETT
PACKARD**

CIRCLE NO 35



SHOWN ACTUAL SIZE

Simultaneous interactive waveforms, alphanumerics and high speed graphics...

ALL IN ONE INSTRUMENT... ONLY FROM GULTON.

The Gulton Supertrak® recorder family combines a graphic plotter, a high-speed line printer and an analog digitized recorder in a single compact module. Choose one to four channels of high quality real time waveform recording with all of these features:

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- High-speed multiple tab-over control in raster graphics for maximum throughput at high chart speeds.
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The Supertrak family of printer/plotter/recorders from Gulton advances the display capability of your medical or industrial instrumentation. Find out more about the Supertrak module that best meets your needs. Write GRAPHIC INSTRUMENTS DIVISION, Gulton Industries, Inc., East Greenwich, RI 02818, or call (800) 343-7929.

CIRCLE NO 36



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NATIONAL ANTHEM®

Technology News From National Semiconductor

51

microCMOS

Twice the Speed From 2-Micron, 1ns microCMOS Gate Arrays

National continues to advance state-of-the-art CMOS gate array technology with its 2-micron (actual drawn geometry) SCX-series microCMOS family. These super-high-performance CMOS gate arrays have a typical internal gate delay of 1ns, and output drive capability of 6ma each.

2-micron performance with 3-micron economics

National's CMOS gate arrays have been production-proven over a wide range of densities from 1200 to 6000 gates. Consequently, these 2-micron devices are offered at prices comparable to their 3-micron counterparts while operating at roughly twice the speed.

Complete development support

National provides the latest in customer training, design automation tools and technical support to help streamline your design process.

For example, a complete range of hardware macros lets you choose the functions needed to implement the desired logic. And an extensive selection of "software macros" from National's software libraries enables you to design large 7400 Series logic functions.

These hardware and software macros are supported by National's fully integrated design automation system offer-

ing user-friendly design verification and 100% auto-place-and-route capabilities.

The TLC™ approach - Gate Array development made easy

From identification of a gate array need through successful implementation of the circuit, National's Training, Layout and Consulting group (TLC) has the expertise and the commitment to work closely with you to ensure a smooth, cost-effective development process.

The TLC commitment includes circuit evaluation, training, logic capture, design verification and validation, place-and-route, implementation, and prototype delivery - the entire range of technical resources necessary to produce advanced designs with built-in integrity and economy.

Design entry via workstations

In keeping with National's dedication to full technical support, workstation design-entry for gate array development is now available through Daisy and Mentor.

National offers the production-proven 2-micron CMOS gate arrays combined with workstation support, expert service, and a comprehensive set of design automation tools. Expect nothing less from the gate array technology leader.

For more information check box M0 on this month's coupon.

Inside News

CMOS

microCMOS Offers New Dimension to VLSI. Over 350 Products Detailed in New CMOS Databook.

Single-Chip microCMOS Modems. Versatile, No-External-Circuitry Converter. Easy Interface with Microprocessor-Compatible Real-Time Clock.

NS32032

First true 32-bit microprocessor.

New Products

TMP Family Opens New Terminal Applications. Small PALs Match 25ns Medium PAL Performance.

PLAN. PAL Software for Easier Programming. 5V-Only E²PROM Offers Fast Read Access. Ultimate Performance Budgeting. 1.2V to 15 V Range Covered by Single 10 Amp Regulator.

Quality

Q/R Policy: Communication is Key.



**National
Semiconductor**

microCMOS: High-performance for the VLSI Era

microCMOS

National meets your needs as a system designer today for speed, analog and digital circuitry on the same chip, a wide operating temperature range, high noise immunity, and reliability with microCMOS.

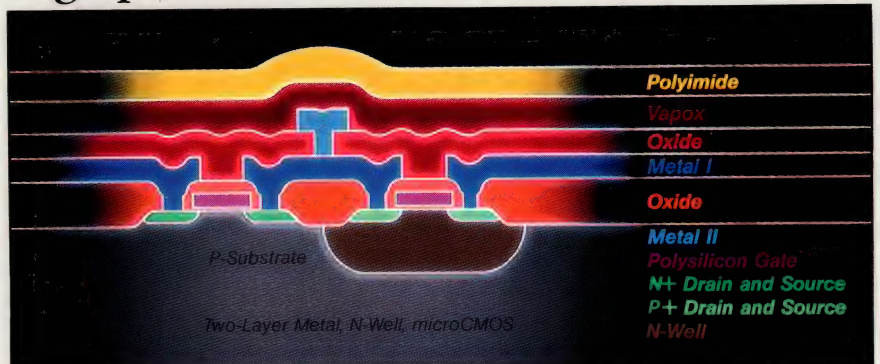
microCMOS is National's array of small geometry, silicon gate, oxide isolated CMOS processes used to manufacture a broad line of more than 250 high-performance integrated circuits.

With low power consumption, microCMOS combines NMOS speed and bipolar ruggedness to begin a new era in VLSI design.

Getting the speed

To increase speed, National uses self-aligning gates and oxide isolation to reduce internal capacitances. Plus, shortened channel lengths and reduced feature sizes throughout the circuit.

National gave speed yet another boost by developing microCMOS in N-well technology. Where extra-high performance is required, multiple-layer, metal interconnect systems extend our speed even further.



Beating the heat

Because microCMOS circuits require only about 5% of the power needed by a comparable NMOS circuit, heat dissipation is much less—allowing many more functions on the same chip.

Unmatched reliability

Proprietary processing enhancements make microCMOS latch-up proof and highly immune to ESD. Low DC current flow decreases metal migration and lower junction temperatures reduce heat dissipation—both of which increase reliability.

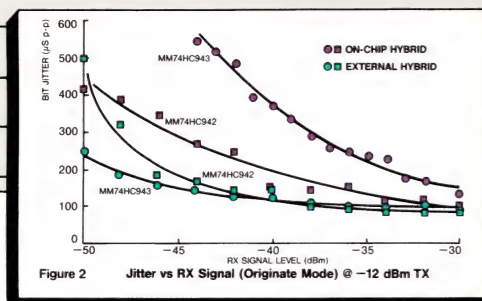
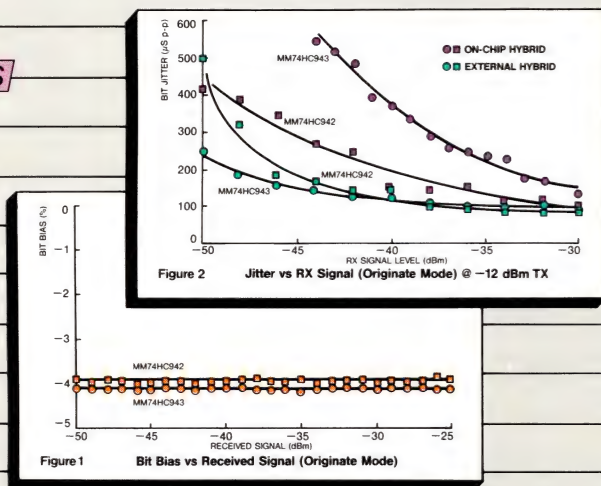
Analog-digital combinations, broad temperature ranges, high noise immunity

The availability of both P and N transistors allows analog and digital circuitry on the same chip. And low power microCMOS chips operate over a wide temperature range. In addition, the large separation between logic voltage levels means high immunity to electrical interference.

Whatever your application, National's more than 250 microCMOS products will help meet your system needs.

For more information, check box **M5** on this month's coupon.

microCMOS



reduced, making significant cost savings possible.

The new modems also incorporate modulator, demodulator and all necessary filtering functions—further reducing required board space.

By simplifying the design and lowering the cost of 300-baud interfaces, the MM74HC942/943 become the practical choice for generating and decoding Bell 103 frequencies.

Lowest bit error rate

When data is modulated by one modem and demodulated by another, two distorting phenomena can occur—bit bias and bit jitter.

Figure 1 illustrates how using National modems results in bit bias typically less than 4 percent. Figure 2 shows the exceptionally low bit jitter of the MM74HC942/943 with on-chip internal hybrid.

When lower-still bit jitter is needed, a simple external hybrid does the job at a small additional cost.

The small size and lower CMOS power requirements allow the MM74HC942/943 to be built directly into computers and terminals, eliminating cumbersome separate units.

For more information, check box **K8** on the coupon in this issue of the Anthem.

New Single-Chip microCMOS 300-Baud Modems

Now available in high-volume production, National's MM74HC942/943 are advanced 0-300 baud microCMOS modems that facilitate data communications between two computers over telephone lines and other narrow bandwidth channels.

The MM74HC943 features a single +5V power supply, while the MM74HC942 further enhances dynamic

range by utilizing a dual $\pm 5V$ supply.

The MM74HC942 dissipates 120mW maximum; the MM74HC943 dissipates 60mW. Both offer a unique power-down mode that can further reduce dissipation to 2.5mW and 1.25mW respectively.

Fewer parts save board space, system costs

National's MM74HC942/943 are the world's first single-chip Bell 103 compatible modems.

Because line driver and hybrid functions are included internally, the number of required parts is substantially

Easy Interfacing and Microprocessor-Compatibility from Real-Time, Clock/Calendar

Accurate time-keeping from tenths of seconds through years

Offering simplified interfacing to microprocessor buses, MM58274 is the latest addition to National's family of low power CMOS clock and calendar devices; which include the MM58167A and MM58174A.

PIN-compatible with the MM58174A, the MM58274 provides extended time-keeping up to units and tens of years plus a variety of added features.



High accuracy at low power

An on-chip 32,768-Hz crystal-controlled oscillator maintains accurate time-keeping with only 10 μ A at 2.2V—allowing low-power standby battery operation and long battery life. Other features include:

- Programmability for 12- or 24-hour operation.
- Interrupts with single or repeat modes for delay times of 0.1, 0.5, 1.0, 5.0, 10, 30 or 60 seconds.
- Easy bus access for both address and data.
- Buffered crystal frequency output for easy oscillator tuning.
- Testable "Data Changed" flag for easy, error-free time reading.

Compact, versatile, economical

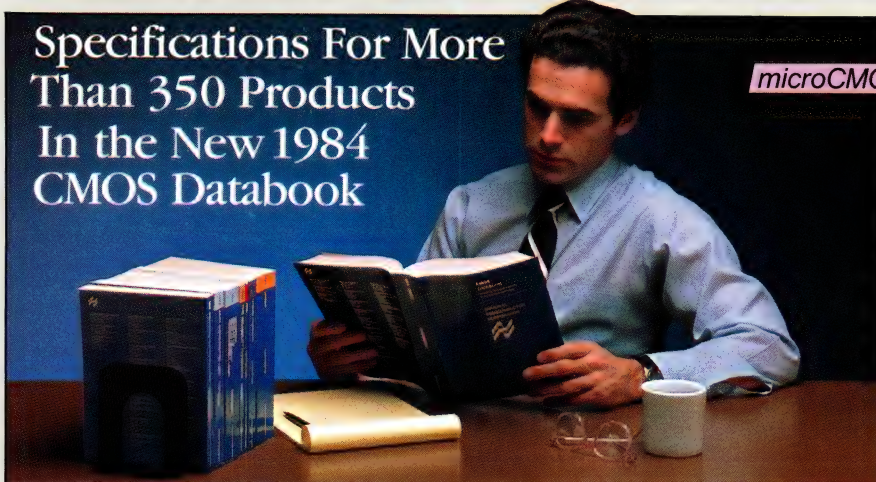
The MM58274 is fully TTL compatible and interfaces without wait states to most microprocessors.

Packaged in a small, 16-pin DIP package, the low-cost MM58274 marks another advance in low-power real-time clock devices for broad applications in bus-oriented microprocessor systems.

For more information, check box **L9** on the coupon in this issue of *Anthem*.

Specifications For More Than 350 Products In the New 1984 CMOS Databook

microCMOS



National Semiconductor Corporation's new CMOS Databook supplies the industry's most comprehensive collection of high-performance CMOS and microCMOS product specifications available today.

This massive reference contains technical information and detailed product specifications on more than 350 products. You'll find yourself referring again and again to this important addition to your technical library.

Our early commitment to microCMOS technology made possible the development of a broad spectrum of advanced devices that will simplify your designs and ensure low-power state-of-the-art systems.

microCMOS technology, National's array of small geometry, silicon gate, oxide-isolated processes was used to build many of the high-performance products described in this 1,500 page databook. Highlights include specifications of the 54/74HC High Speed microCMOS Logic Family, A/D and D/A Converters, CMOS Industrial Microcomputer Boards (CIM™), Telecommunication Devices and much more.

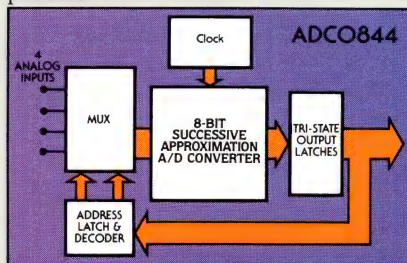
microCMOS accounts for nearly half of National's current research and development effort, and this technological commitment will increase through the 80's.

To order your data book today, refer to this month's coupon.

The Efficient ADC0844 Converter: All You Need Between Incoming Analog Signals and Your Data Bus

μ P compatible too

National's ADC0844 8-bit A/D converter offers a versatile 4-channel analog-input multiplexer complete with built-in address logic and an internal clock. In most cases, no external circuitry is needed for the digitizing process.



Total unadjusted error (including offset, full-scale, linearity and multiplexer errors) is $\pm 1/2$ LSB and ± 1 LSB.

The advanced device is fully compatible with most microprocessors, and operates from a single 5V power supply. Power consumption is a mere 10mW.

Designed to operate from the control bus of the NSC800, the converter incorporates TRI-STATE® output latches that directly drive the data bus. As a result, the unit can be configured as a memory location—or as an I/O device to the microprocessor. No interface logic is needed.

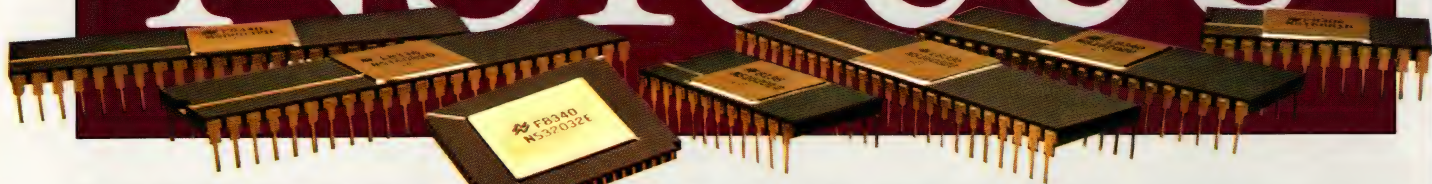
The ADC0844 operates ratiometrically or with 5V_{DC} voltage reference, 0V to 5V input range with single 5V power supply, and delivers a rapid conversion time of just 40 μ s (max.)—all in a 0.3" standard width 20-pin DIP!

The 4-channel multiplexer of the ADC0844 can easily be software-configured for single-ended or differential operating modes—or any combination of the two.

For these reasons, the versatile ADC0844 converter is your high-efficiency design choice.

For complete details, check box **J0** in the coupon on back page.

NS16000



NS32032

With the recent introduction of NS32032, National's NS16000 microprocessor family has become the foundation for the next generation of high performance, low cost computers.

The new microprocessor is the first to feature:

- Full 32-bit architecture
- Full 32-bit internal implementation
- Full 32-bit data bus to memory

Any software developed for the 32-bit NS32032 will run just as well on the 16-bit NS16032 or the 8-bit NS08032, and vice-versa. It will also run on future 32-bit CPU versions.

Downward/upward compatibility

The absolute *downward-upward* compatibility of the NS16000 CPU family is in sharp contrast to the *upward-only* compatibility of other microprocessor families. Their 16-bit processors will become obsolete when 32-bit processors join their product lines.

The fact that National's NS08032 and NS16032 CPUs (with their 8-bit and 16-bit data buses) share identical 32-bit architecture and 32-bit implementation with the NS32032, means it is now possible to develop 8- and 16-bit systems with all the benefits of 32-bit software performance.

The same software can now be implemented on all systems within a product family – an enormous benefit to programmers and systems designers. **NS32032 is supported by available peripherals**

The NS16000 family already includes all these peripherals: the NS16201 Timing Control Unit, the NS16202 Interrupt Control Unit, the NS16081 Floating Point Unit, and the NS16082 Memory Management Unit – all in full production now.

National's 32-Bit Microprocessor Joins the Impressive NS16000 Family

Mainframe software on microprocessor-based systems. Another industry 'first'

The billions of bytes of existing mainframe software can now be easily ported to run on NS16000-based systems.

This achievement is an industry 'first', made possible by NS16000's architectural support for high level language programming, its full high-speed floating point arithmetic capability, its integral support for Demand Paged Virtual Memory, and the NS32032's 32-bit data bus to memory.

Microprocessor speeds from 1 MIPS to 10 MIPS

Future 32-bit CPU versions from National will also be compatible, ranging from the 1 MIPS NS32032 today to 10 MIPS by 1988. The migration path

for product enhancement will be clear, and the initial software investment of National customers will be preserved.

Fully implemented 32-bit architecture, without exception or restriction

The value of elegant implementation is easily illustrated. Except for NS32032, every microprocessor available today takes eight to 20 internal steps to execute the equation: $A = A \cdot X + A_i$, an expression evaluation commonly used in technical and scientific applications.

The NS32032 takes four.

To better understand the significance of this milestone in computer technology, order your free copy of NS16000: The Specifics of 32-bit Architecture. Check box L6 in this Anthem's coupon.

Now compiled in one book for fast easy reference

The Elegant NS16000 Microprocessor Family

All hardware, software and development-tool data sheets

More than 500 pages in all! Includes specs, instruction sets and architectural descriptions of the three CPU families: (NS08032, NS16032 and NS32032); plus memory management, floating point, and 10 peripherals.

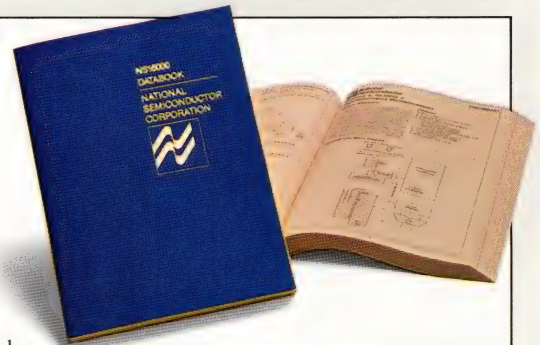
Also featured is information on the supporting development tools and software – the SYS16™, ISE16™, DB16000, cross software, and GENIX™ operating system.

GENIX, a version of Berkeley 4.1 bsd UNIX™ tailored for the NS16000 family,

supports Demand Paged Virtual Memory and optimizes the 16000 architectural elegance. GENIX runs on SYS16 and is available in source code form for OEM adaptation to NS16000-based systems.

Don't miss this important industry publication – an information bonanza at the reduced price of only \$5.00 each.

To order, check box L5 on this Anthem's coupon and return with your remittance. Multiple-copy orders welcome!





New, Simpler, 20-Pin Small PALs Match 25ns Medium PAL Performance and Cost Less

For over a year, designers of high performance digital systems have taken advantage of the 25ns Medium PAL Family to replace LS Logic devices in their systems. Now, the same performance advantage is available in the 20-Pin Small Family—a less complex, less costly family—from National Semiconductor.

Address decoding, multiplexing, arbitration, and high-speed random gating are typical applications which can be made faster by replacing low power Schottky SSI gates with National's new high-speed PAL® devices.

Integration improves system development

Designing with National's new PAL family enables you to reduce your chip count, typically by 4:1 to achieve significant space and cost savings. Improved system reliability from fewer components are added benefits.

Design flexibility and simplicity through instant customization

Beyond the obvious advantage of flexibility obtained from the ability to program chips to perform specific functions, PAL technology simplifies the



design process. Simplification is primarily due to the automated design capability offered by PLAN™—National's new design software.

In addition, complex interconnections that previously required time-consuming PC layout are now processed in silicon where they can be easily modified during prototype checkout or production.

More design and product benefits

Additional design benefits of National's PAL family include variable input/output

ratio, skinny DIP packages for more compact designs, and titanium-tungsten fuses for greater reliability.

Moving you ahead

Higher speeds and the many other benefits of PAL technology help make your designs as advanced as they can be.

For shortening your product's design-to-market cycle, there's nothing faster and more efficient in programmable logic circuits than National's new PAL devices.

For more information, check box P6 on the Anthem coupon.

PLAN™ Makes PAL Programming Easier Than Ever

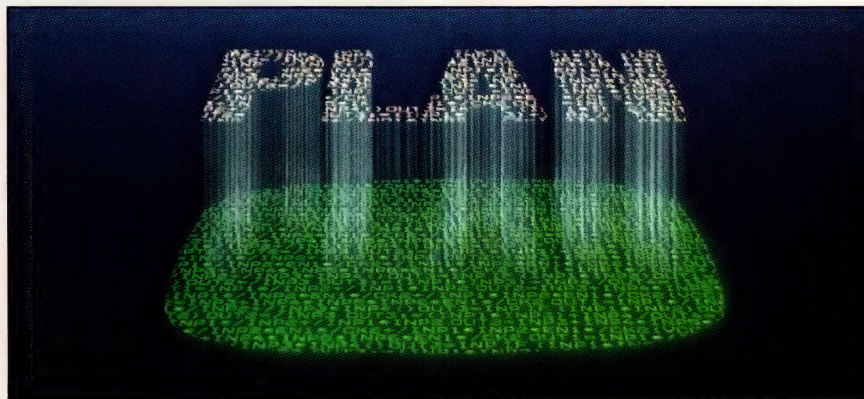
PLAN (Programmable Logic Analysis by National) is a set of interactive design and development tools specifically created for systems designers using PAL (Programmable Array Logic) devices.

These tools take the errors and confusion out of determining PAL requirements; they automatically select the correct PAL, saving valuable time spent in search and evaluation.

PLAN's primary programs, 'PLUS', 'PROG' and 'SERV' guide designers all the way from initial Boolean entry, through device selection and documentation, to the programming of the devices on DATA I/O and other programmers.

Efficient, versatile

Interfacing with virtually all popular PAL programmers, and using notations like those of the familiar PALASM®, PLAN accepts Boolean equations and provides on-going message to the user regarding PAL requirements for the



equations. And PLAN's comprehensive messaging includes error alerts, device selection guidance and prompts.

Next, PLAN *automatically* selects the proper PAL—and the pin assignments—and creates a permanent file on disk representing the defined logic element.

Easy to use

PLAN offers design engineers a more friendly method of operation. Displaying equations, for example, is as easy as entering 'STATUS' and providing an affirmative response to PLAN's subsequent question.

If, after automatic PAL selection, the user has reason to believe that a

different PAL would serve better, PLAN can be instructed to evaluate any PAL of the user's choice for implementing the set of equations at hand.

Designed to work with a broad range of personal computers, PLAN is supplied on 8-inch single-side, single-density disks formatted for operation under CP/M-80® and on 5-1/4-inch single-side, double density floppy disks for operation under MS-DOS®.

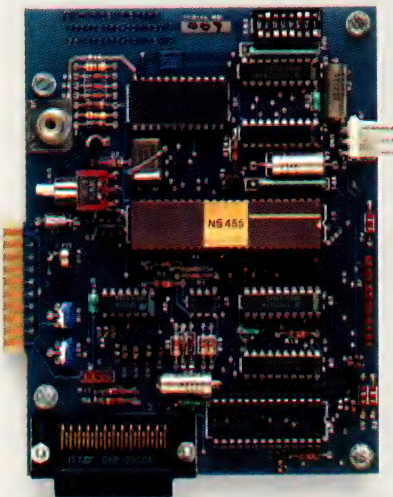
PLAN. One more powerful tool from National for the system designer.

For complete information, check Box K7 in the coupon on back page.

NEW PRODUCTS

CRTs Are No Longer Limited To Traditional Terminal Applications

If your application could benefit from a CRT data display but you don't have the space, there is now a device that gives you full CRT functions on a smaller board.



The small size of the NS455 Series TMP Evaluation Board allows many new CRT applications.

National's amazing new NS455-Series Terminal Management Processor (TMP) family provides the functions of an 8-bit microprocessor, CRT controller, ROM, DMA controller, character generator, UART and BAUD rate generator in one 48-pin package. The integration provided by the TMP offers board area savings, improved reliability and faster design cycles.

See how small a complete system can be

The NS455 evaluation board typifies the type of minimum CRT data terminal system possible with a pre-programmed TMP. With the addition of a video monitor, ASCII-encoded keyboard, and power supply, a complete data terminal is structured. In addition, you may write your own program, which the NS455 can execute by using external program memory (up to 8K offboard).

Features of the TMP evaluation board include:

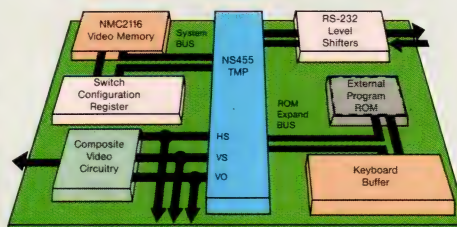
- Internal masked ROM or external EPROM program execution
- 80 column x 25 row display
- 5 x 7 characters with 2 level descenders
- 12 MHz video bandwidth

- BALL or composite video output
- 50/60 Hz operation
- RS-232C Serial Interface with Full Duplex 110-19.2K BAUD
- Status line display
- 24 escape sequences
- 15 control sequences

Familiar instruction set makes programming easy

Feel comfortable right away with the chip's familiar, but enhanced, 8048 instruction set. The system operates with two, bidirectional buses—a 16-bit system bus providing up to 64K by 16 bits of video RAM addressing, and a 13-bit ROM expansion bus offering up to 8K of addressing, all off-chip, or 2K on and 6K off-chip.

National offers a complete selection of boards and devices for your system design. Eliminate software design efforts by continuing to use the NS455 evaluation board or the pre-programmed NS455 found on it. Or develop your own program with the NS405 ROMless device. And for higher volume quantities, the program can be masked into the NS456.



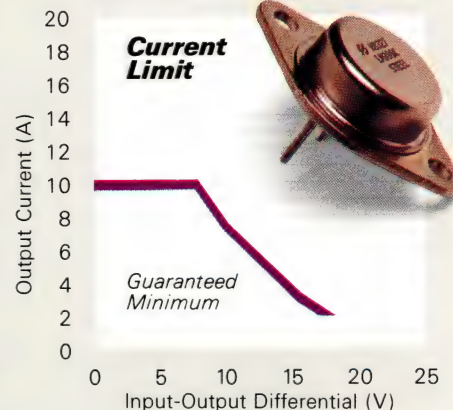
New MOLE™ Development System makes TMP design-in and program development easy

The MOLE (Microcontroller On-Line Emulator), National's low-cost development system, brings dedicated support to the TMP chip with the MOLE Brain board, Personality board and software package.

The high-speed processing and storage capabilities of your host computer and MOLE software provide the ability to program, edit and cross-assemble the TMP program. The results are then downloaded over an RS-232C link to the MOLE boards where real-time in-circuit-emulation and program debugging take place in a free-standing, workstation mode. The result is rapid program development capability using your familiar host computer system. MOLE also supports other members of National's microcontroller family.

For more information, check Box M6 on the response coupon on the back page.

A Single, 10 Amp Voltage Regulator Meets Output Specs From 1.25V to 15V



This is the voltage regulator for all your 10 amp designs. With National's LM396 there's no need to design-in several lower current regulators for one voltage application requiring output from 1.25V to 15V. The LM396 is easy to use and continuously adjustable.

The LM396 Adjustable Voltage Regulator enhances system performance, reduces the system part count requirement, and increases reliability beyond any regulator currently available.

Consistency and protection in worst cases and conditions

The LM396 ensures 10 amp output current under worst-case conditions. Running at power levels up to 70 watts, the output voltage will remain as set. The LM396 is immune to blowout from overloads, shorts, or accidental disconnection of the adjustment pin.

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The LM396 features on-chip trimming of reference voltage to $\pm 0.8\%$.

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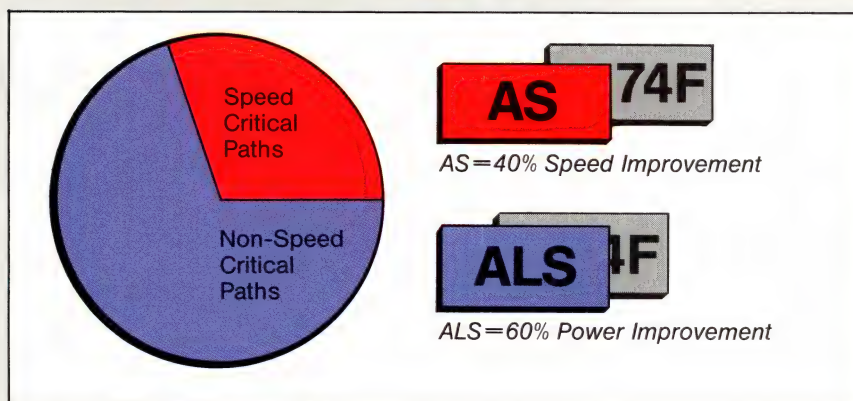
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Successful Communication Ensures Products That Work

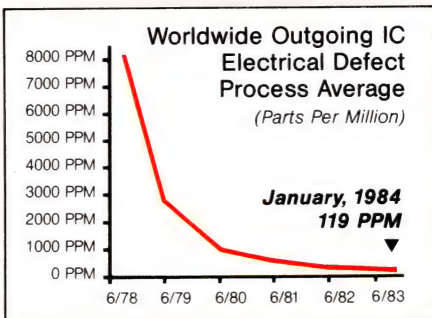
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- M0 ☐ Gate Array Brochure
- M1 ☐ AS/ALS Performance Budgeting Brochure
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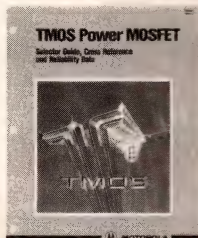
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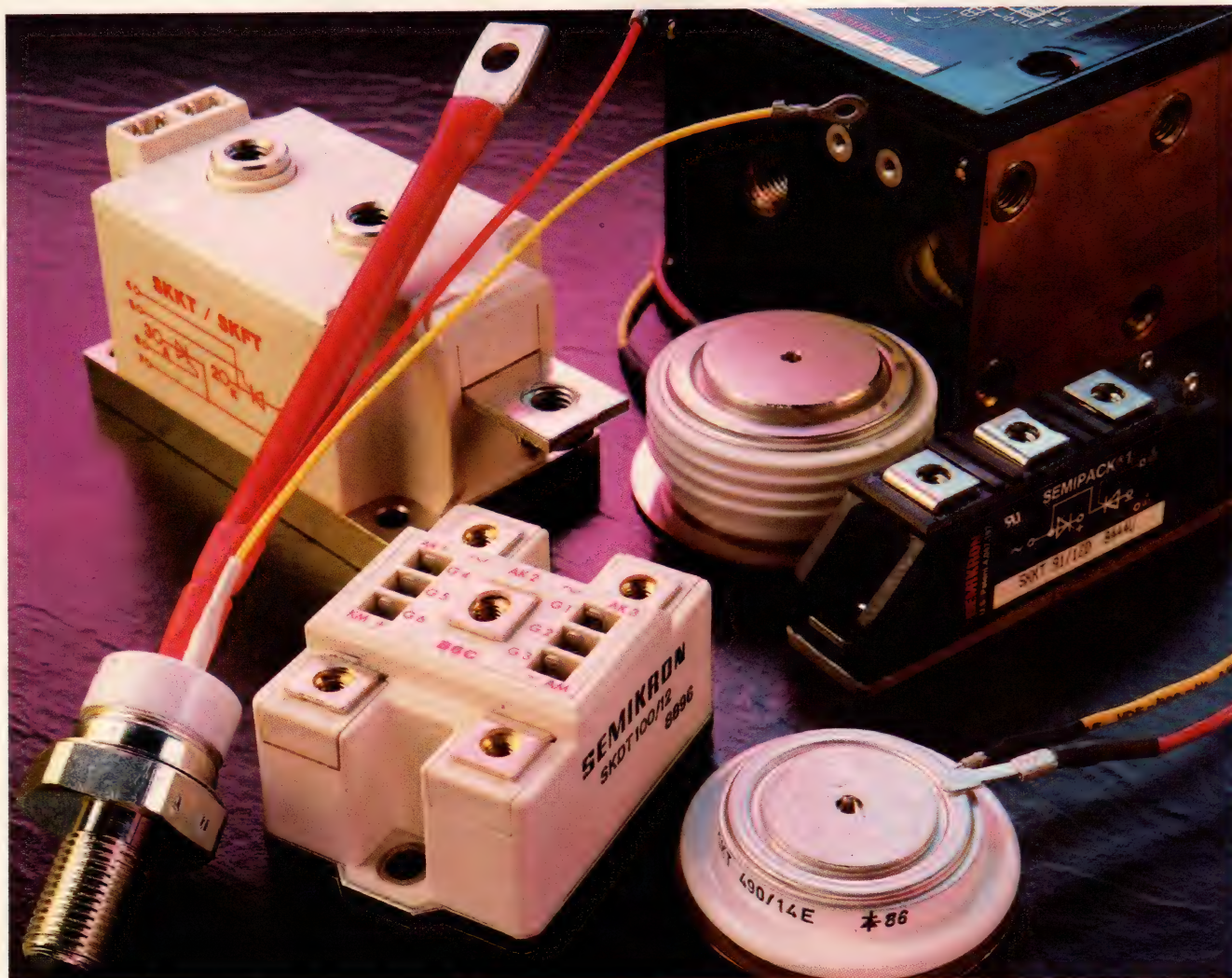
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CIRCLE NO 37

TECHNOLOGY UPDATE

Gate-turn-off thyristors spec new current/voltage highs

Peter Harold, *European Editor*

Gate-turn-off (GTO) thyristors are replacing silicon controlled rectifiers (SCRs) as solid-state switches in high-frequency power-conversion equipment. GTO thyristors are now available with voltage ratings as high as 4.5 kV. By eliminating the need for the bulky and expensive LC networks required to commutate equivalent SCRs, the devices allow reductions in size, weight, and manufacturing cost. Be aware, however, that their more complex gate waveforms increase drive-circuit complexity.

The production of high-power GTO thyristors owes much to techniques originally developed for VLSI-device fabrication. The gate/cathode structure of a GTO thyristor must be highly interdigitated in order to minimize switching times, ensure adequate turn-off gain in the device, and control avalanche breakdown during the turn-off period.

Fabricating this structure necessitates the use of fine-line lithography to produce patterns clean enough to avoid field-strength breakdown, and the use of such techniques as neutron-transmutation doping to adequately control silicon resistivities and thereby ensure current sharing among the multiple cathodes.

The availability of these techniques has increased the number of manufacturers prepared to produce GTO thyristors. Current product offerings range from TO-220-encapsulated devices capable of switching a few amps, to giant hockey-puck GTO thyristors that can repeatedly switch 2500A at voltages as high as 4.5 kV.



Generating all the necessary gate waveforms, International Rectifier's driver modules enable you to control 81- and 84-RDT stud-mounting GTO thyristors and 160PFT pressure-pack GTO thyristors with a single logic level.

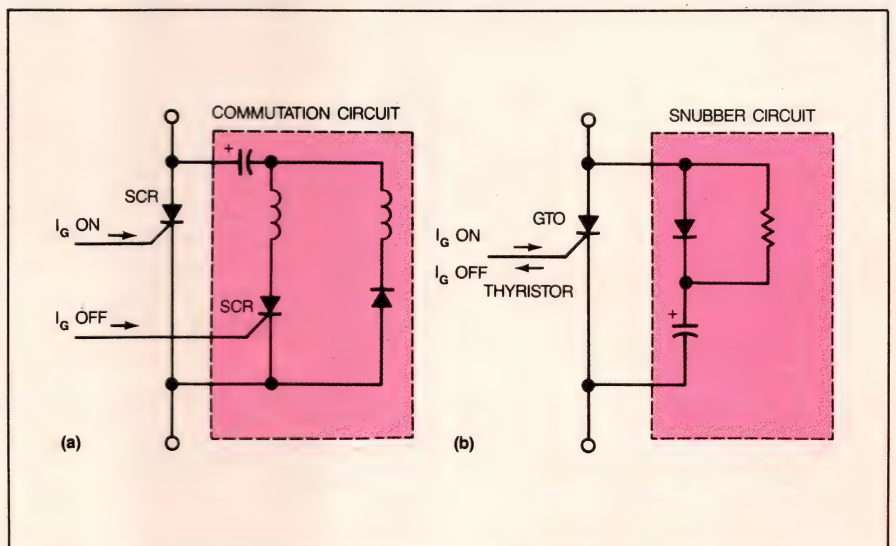
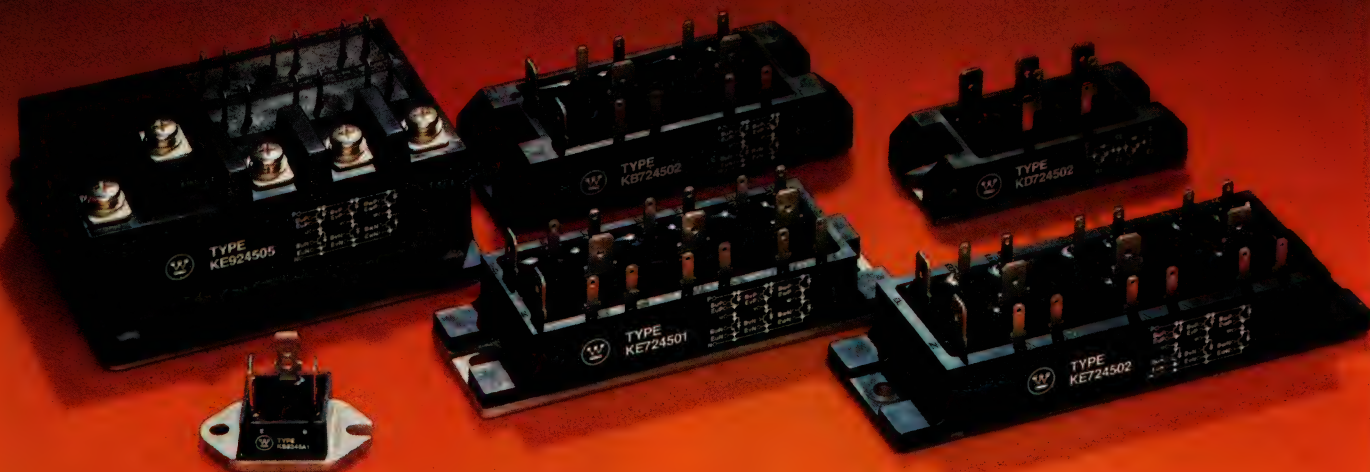


Fig 1—The snubber components required by the GTO thyristor in circuit **b** are far less bulky and expensive than the SCR's commutation components in circuit **a**.

New additions to the Darlington line.



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Taking a look at the lower end of voltage and current ratings, GTO thyristors switching less than 400A and having forward-voltage capabilities below 1 kV encounter fierce competition from the new generation of bipolar power transistors. In comparison with GTO thyristors, bipolar transistors have simpler base-drive requirements and lower on-state saturation voltage, and they allow you to operate at frequencies above the GTO thyristors' 1- to 2-kHz limit.

Nevertheless, if your application involves high peak-to-average current ratios, eg, those encountered in pulse-width-modulated (PWM) inverters or under fault conditions, GTO thyristors probably still fare better than bipolar transistors. Because the self-regenerative switching action of the GTO thyristor forces it further into saturation as the anode current increases, the device does (for a given average current) carry and switch higher peak currents than a bipolar transistor.

High- and medium-power GTO thyristors (Tables 1 and 2) frequently replace SCRs in such appli-



This 50-mm GTO thyristor wafer from Marconi Electronic Devices Ltd shows the highly interdigitated gate/cathode structure of a gate-turn-off thyristor.

cations as dc-to-dc chopper converters, uninterruptible power supplies, and 3-phase, variable-speed, ac-motor-drive inverters. Because a GTO thyristor turns off through the extraction of a current pulse from its gate electrode, the device eliminates the need for the large inductive and capacitive components necessary to reduce artificially an SCR's anode current to zero and, by so doing, commute it to the off state (Fig 1).

Electromagnetic and acoustic noise, associated with high-current

switching in the commutation circuit, is also lower for a GTO thyristor. A typical device is capable of breaking a current two to three times its rms load current. Although you require larger snubber circuits to adequately control the GTO thyristor's anode dV/dt (occurring immediately after turn-off) and more complex gate-drive circuitry, the added cost of these circuits is exceeded by the savings in cost, size, and weight achieved by eliminating commutation components.

Consider gate-drive circuitry

Fig 2 illustrates the typical gate-control waveforms required to turn a GTO thyristor on and off. Turning on a GTO thyristor is much the same as turning on an SCR, ie, by applying a positive current pulse to the gate electrode. However, unlike the case of the SCR, the GTO thyristor's rate of rise of gate current (dI_G/dt) is critical to ensure a fast turn-on time and good dynamic current sharing in the multiple cathodes.

Unless you're certain that anode current will be maintained at a sufficiently high level, you must continuously supply a small level of gate current (back-porch current) during the GTO thyristor's on period. Without this sustained gate current, an unpredicted fall in anode current could cause some cathodes to unlatch into the off state—imposing an excessive current density on those cathodes that remain latched—when the anode current rises again.

Because of their interdigitated cathode structure, GTO thyristors exhibit rapid turn-on times of 5 to 10 μsec typ. The devices can therefore sustain a high rate of rise of anode current: A rate as high as $600\text{A}/\mu\text{sec}$ is permissible for some devices.

Turning off a GTO thyristor is more difficult. Turn-off gain in high-current devices is usually around 5, so to break a load current of 2500A requires that you extract a 500A current pulse from the gate. In ad-

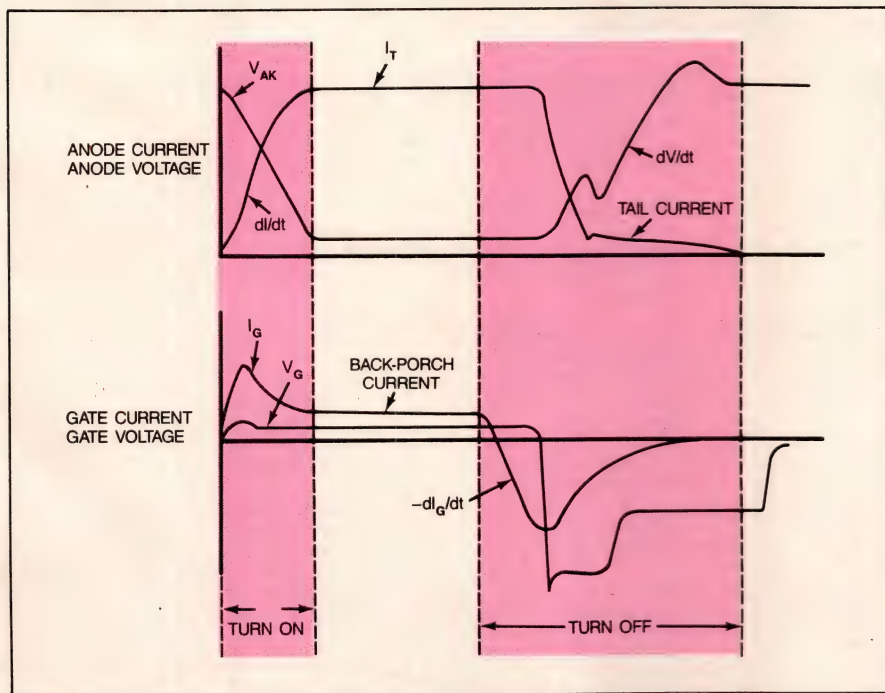


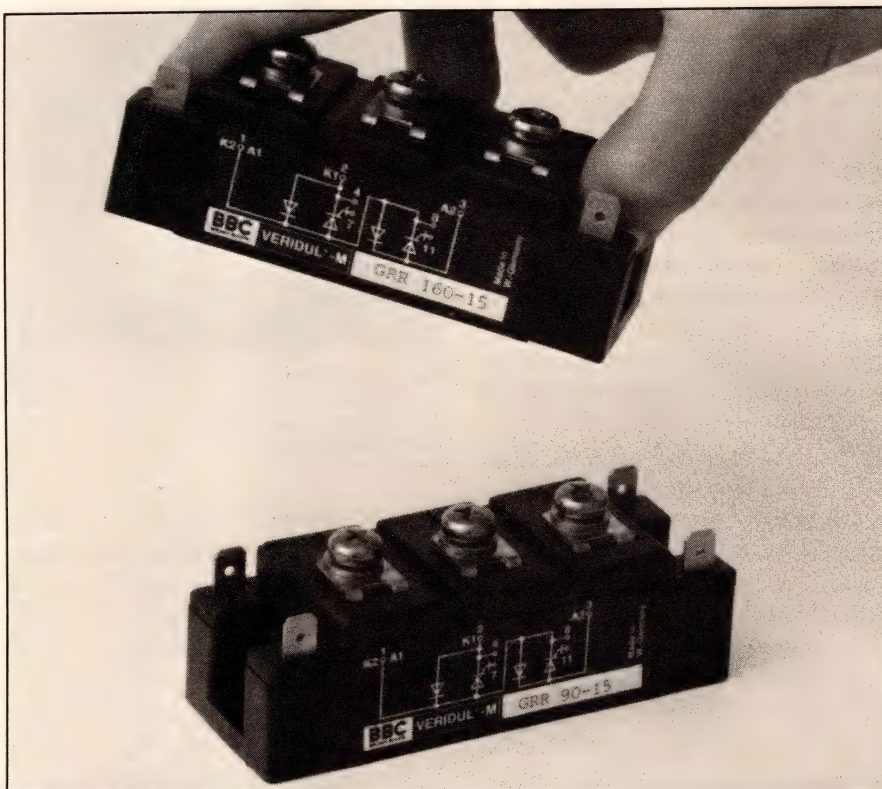
Fig 2—Defining gate-drive waveforms for a GTO thyristor requires a thorough understanding of device and load parameters in order to minimize switching losses.

TECHNOLOGY UPDATE

dition, you must control the rate of rise of gate current (usually by controlling the gate circuit's inductance) to optimize turn-off time and power losses in the GTO thyristor.

However, for those who don't wish to become involved in the complexities of gate-drive circuitry, several companies offer gate-drive modules for their GTO thyristors. Typical of these are International Rectifiers' GK2-A and -B modules, which drive the firm's 81/84-RDT and 160PFT GTO thyristors, respectively. The modules reduce GTO-thyristor on-off control to a 12V logic level, provide 2.5-kV optical isolation between the control input and the GTO thyristor, and require only a +5 and -15V dc power supply with reference to the GTO thyristor's cathode.

A possible disadvantage of using a manufacturer's drive module, though, is that you might not be able to optimize the gate drive to suit particular load conditions. For



Typical of GTO-thyristor modules, the GRR-90 and soon-to-be-released GRR-160 from BBC Brown Boveri are easy to mount; moreover, they provide electrical isolation from the heat-sink assembly.

For more information . . .

For more information on the gate-turn-off thyristors described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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example, consider a particular situation in which you activate a single-shot, artificially high gate-current pulse to turn off a fault load current.

After the bulk of a GTO thyristor's anode current turns off, a low-level tail of anode current continues to flow for a period of time, as a result of charge storage in the GTO thyristor's n-base regions. Alternative measures taken to minimize the duration of this tail current—and hence to minimize the total turn-off time—resulted in the manufacture

of two types of GTO thyristors.

If you dope the n-base region with a heavy metal (eg, gold), a technique that provides recombination centers for trapped charge, you end up with a symmetric GTO thyristor capable of blocking approximately equal forward and reverse voltages. The alternative method—providing a recombination circuit by shorting out the n-base region to the anode-emitter metallization—results in an asymmetric GTO thyristor.

This asymmetric GTO thyristor

has severely limited reverse-voltage blocking capability: typically below 20V. You therefore need to provide some form of protection unless you can guarantee that this blocking-voltage value is never exceeded. The advantage of the anode-emitter shorting method is that it lowers the device's on-state voltage, and hence the on-state power loss, by 10 to 15%.

For switching currents as high as 200A, many manufacturers offer GTO-thyristor modules, which in-

TABLE 1—HIGH-POWER GTO THYRISTORS (HOCKEY-PUCK PRESSURE PACKAGES)

MANUFACTURER	TYPE NUMBER	REPETITIVE PEAK OFF-STATE VOLTAGE	RMS ON-STATE CURRENT	REPETITIVE PEAK CONTROLLABLE ON-STATE CURRENT	SURGE (NON REPETITIVE) ON-STATE CURRENT
		V_{DRM} (V)	I_T (RMS) (A)	I_{TCM} OR I_{TGO} (A)	I_{TSM} (A)
HITACHI	GFP600B12	1200	220	600	4500
	GFP600C16	1600	270	600	6000
	GFP1000B25	2500	400	1000	7000
	GFP2000B25	2500	800	2000	—
INTERNATIONAL RECTIFIER	150PFT-200,-250	2000,2500	235	800	2100
	160PFT-100,-120	1000,1200	250	600	2600
	160PFT-140,-160	1400,1600	250	600	2100
	160PFT-100A,-120A	1000,1200	250	700	2600
	320PJT-200,-250	2000,2500	450	1500	—
	350PJT	1000-1600	550	1200	4700
MARCONI ELECTRONIC DEVICES	DG224SE	1200	120	300	2000
	DG304SE	1200	250	600	4000
	DG386SL	2500	400	1000	7000
	DG506SD	2500	600	1400	12000
	DG508SD	4500	500	1800	10000
	DG758SU	4500	800	2500	16000
MITSUBISHI ELECTRIC	FG450BL	800-1600	200	450	2500
	FG600AL	800-1600	270	600	5000
	FG600AH	2000,2500	270	600	5000
	FG600C	2000,2500	270	600	5000
	FG1000A	2000,2500	450	1000	7000
	FG1000AL	800-1600	450	1000	7000
	FG1000AH	2000,2500	450	1000	7000
	FG1800AH	2000,2500	860	1800	11000
	FG2000AV	4500	700	2000	7000
TOSHIBA	SG600R21	1300	400	600	—
	SG800R21	1300	400	800	—
	SG1000R22	1300	250	1000	—
	SG600EX21	2500	400	600	—
	SG800EX21	2500	400	800	—
	SG1200EX21	2500	700	1200	—
	SG1400EX21	2500	700	1400	—
	SG2000EX21	2500	1000	2000	—
	SG400EX22	1300-2500	150	400	—
	SG500GXH22	3300,4500	200	500	—
	SG700EX22	1300-2500	200	700	—
	SG800GXH22	3300,4500	300	800	—
	SG1000EX23	1300-2500	400	1000	—
	SG2000EX22	1300-2500	800	2000	—
	SG2500GXH22	3300,4500	800	2500	—
	SG2700EX22	1300-2500	1000	2700	—
WESTINGHOUSE	GSO11245	1200	200	450	2500
	GSO11260	1200	270	600	5000

*POR—PRICE ON REQUEST

TECHNOLOGY UPDATE

corporate two series-connected GTO thyristors or a combination of a GTO thyristor and power diodes, in configurations suitable for direct use in bridge circuits. **Table 3** highlights the diversity of circuit configurations available.

These modules typically offer 2.5-kV isolation between the internal GTO-thyristor pellets and their base plate, and they allow you to easily mount several devices on one heat-sink assembly.

This ease of mounting, however,

is not a feature of higher-current GTO thyristors. With the exception of some flat-base devices from Toshiba, GTO thyristors capable of switching over 400A are packaged in hockey-puck pressure packages whose faceplates form the anode and cathode electrodes. Not only do you have to ensure even contact between these faceplates and the connection/heat-sink assemblies, but you must also clamp the GTO thyristor between the two assemblies with a specified force while

maintaining anode-to-cathode isolation.

The GTO thyristor market is now seeing increased competition from European vendors. AEG-Telefunken, BBC Brown Boveri, Marconi Electronic Devices, and Philips are offering varied products (see **Tables 1, 2, and 3**). In late 1985 and 1986, moreover, you'll see other companies entering the field.

Siemens, which estimates a 15% annual growth rate in the market for GTO thyristors and fast thyris-

Text continues on pg 70

	CRITICAL RATE OF RISE OF ON-STATE CURRENT	CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE	REPETITIVE PEAK REVERSE VOLTAGE	ON-STATE VOLTAGE	REPETITIVE PEAK OFF-STATE CURRENT	GATE-CONTROLLED TURN-OFF TIME	PRICE
	di/dt (A/ μ SEC)	dV/dt (V/ μ SEC)	V _{RRM} (V)	V _{TM} AT I _{TM} (V) (A)	I _{DRM} (mA)	t _{GO} (MAX) μ SEC	
	100	600 TYP	—	2.0 450	50	7	POR*
	200	600 TYP	—	2.5 600	50	15	POR*
	260	600 TYP	—	2.5 1000	50	30	POR*
	—	—	—	2.5 —	—	35 TYP	POR*
	500	1000	2000,2500	3.2 471	80	15	\$1425 ALL PRICES
	600	1000	1000,1200	2.7 503	50	8	\$400 ARE FOR A
	600	1000	1400,1600	3.15 503	50	8	POR* 1200 OR
	600	1000	1000,1200	2.7 503	50	8	POR* 2000V V _{RRM}
	—	—	2000,2500	2.8 900	—	15	\$2275 (1 to 9)
	600	1000	1000-1600	3.42 1100	80	15	\$963
	500	500	16	2.5 300	25	10 TYP	~\$130 (1000)
	500	500	16	2.5 600	50	10 TYP	~\$290 (1000)
	250	500	16	2.5 1000	50	20	~\$730 (100)
	250	500	16	2.5 1400	100	25 TYP	~\$1900 (10)
	250	500	16	3.0 1800	100	100 TYP	POR*
	250	500	16	3.0 2500	200	50 TYP	POR*
	200	500	15	2.5 450	60	15	~\$250
	200	500	15	2.2 600	80	15	~\$300
	200	500	15	2.5 600	80	20	POR*
	200	500	500	3.2 600	80	20	POR*
	200	500	500	3.5 1000	100	20	POR*
	200	500	15	2.2 1000	100	15	~\$550
	200	500	15	2.5 1000	100	20	~\$600
	300	500	15	3.0 1800	120	30	~\$1500
	300	1000	15	3.5 2000	150	30	POR*
	100	350	650	2.0 600	50	18	por*
	100	350	650	2.0 800	50	18	por*
	200	350	100	2.8 1000	50	15	por*
	100	350	1250	2.3 600	50	18	por*
	100	350	1250	2.3 800	50	18	por*
	250	350	500	2.5 1200	100	22	por*
	250	350	500	2.62 1400	100	25	por*
	—	—	—	2.5 —	—	23	por*
	200	400	15	2.5 400	10	16	por*
	200	500	15	3.5 500	40	15	por*
	150	400	15	2.7 700	10	16	por*
	200	500	15	3.5 800	40	15	por*
	250	400	15	2.5 1000	20	18	por*
	300	500	15	2.8 2000	50	23	por*
	300	500	15	3.5 2500	150	25	por*
	300	500	15	3.0 2700	60	25	por*
	200	500	15	2.5 450	60	15	\$200 (250)
	200	500	15	2.2 600	80	15	\$275 (25)

TECHNOLOGY UPDATE

**TABLE 2—MEDIUM-POWER GTO THYRISTORS
(STUD-MOUNTED AND FLAT-BASE PACKAGES)**

MANUFACTURER	TYPE NUMBER	REPETITIVE PEAK OFF-STATE VOLTAGE	RMS ON-STATE CURRENT	REPETITIVE PEAK CONTROLLABLE ON-STATE CURRENT	SURGE (NONREPETITIVE) ON-STATE CURRENT
		V_{DRM} (V)	I_T (RMS) (A)	I_{TCM} OR I_{TGO} (A)	I_{TSM} (A)
AEG-TELEFUNKEN	G20A	1200	10	20	44
	G50A	1200	22	50	125
	G90A	1200	40	90	270
	G200A	1200	—	200	330
HITACHI	GFT20B12	1200	7	20	65
	GFT50B12	1200	18	50	180
	GFF90B12	1200	30	90	400
	GFF200E12	1200	70	200	500
	GFF300E12	1200	100	300	700
INTERNATIONAL RECTIFIER	81RDT-100M,-120M	1000,1200	125	350	1550
PHILIPS	BT157-1300,-1500	1300,1500	3.2 AVG	12	20
	BTV59-600,-850,-1000	600-1000	15 AVG	50	100
	BTV60-850,-1000,-1200	850-1200	25 AVG	120	150
TOSHIBA	SG300EX11	1300-2500	120	300	2640
	SG400EX11	1300-2500	150	400	3300
	SG700EX11	1300-2500	200	700	4400
	SG800EX11	1300-2500	300	800	6600

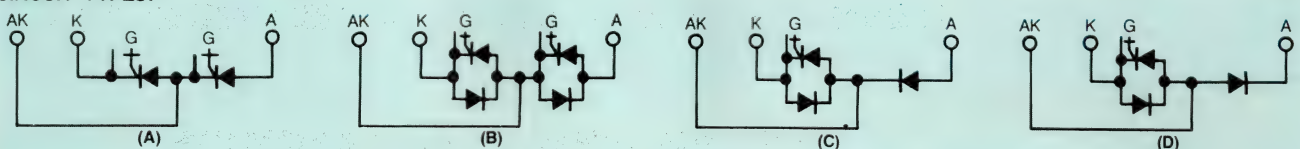
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TABLE 3—GTO-THYRISTOR MODULES

MANUFACTURER	TYPE NUMBER	CIRCUIT TYPE	REPETITIVE PEAK OFF-STATE VOLTAGE	RMS ON-STATE CURRENT	REPETITIVE PEAK CONTROLLABLE ON-STATE CURRENT
			V_{DRM} (V)	I_T (RMS) (A)	I_{TCM} OR I_{TGO} (A)
AEG-TELEFUNKEN	GG50,GD50,DG50 SERIES	A,B,C,D,E,F	1200	22	50
	GG90,GD90,DG90 SERIES	A,B,C,D,E,F	1200	40	90
	GG150,GD150,DG150 SERIES	A,B,C,E	1200	60	150
BBC BROWN BOVERI	GRR90	B	800-1500	48	90
MARCONI ELECTRONIC DEVICES	MGT100D-120	B	1200	31	100
	MGT150D-120	B	1200	50	150
MITSUBISHI	GM100DY	B	800-1200	31	100
	GM200DY	B	800-1200	70	200
TOSHIBA	S6418	B	1200,1300	30	50
	S6419	B	1200,1300	50	100
	S6420	G	1200,1300	90	200
WESTINGHOUSE	GDM-11210,-21210	A,B	1200	31	100
	GDM-11220,-21220	A,B	1200	70	200

**POR—PRICE ON REQUEST * TYPES WITHOUT ANTIPARALLEL DIODES.

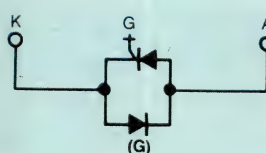
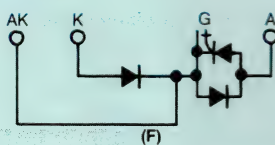
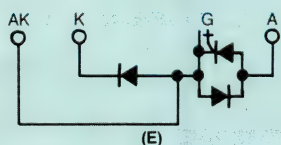
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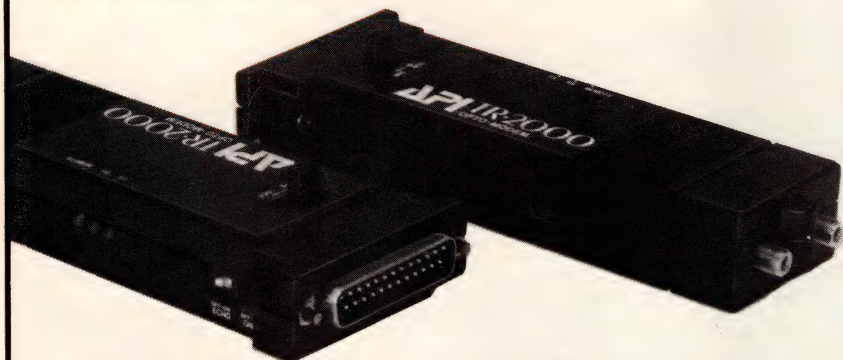
TECHNOLOGY UPDATE

CRITICAL RATE OF RISE OF ON-STATE CURRENT	CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE	REPETITIVE PEAK REVERSE VOLTAGE	ON-STATE VOLTAGE	REPETITIVE PEAK OFF-STATE CURRENT	GATE-CONTROLLED TURN-OFF TIME	PRICE
di/dt (A/ μ SEC)	dV/dt (V/ μ SEC)	V_{RRM} (V)	V_{TM} AT I_{TM} (V) (A)	I_{DRM} (mA)	t_{GQ} (MAX) μ SEC	
150	1000	13	3.35 20	3	6	POR*
200	1000	13	3.45 50	5	6	POR*
200	1000	13	3.1 90	8	6	POR*
200	1000	13	4.1 200	—	6.5	POR*
150	1000	—	3.0 20	1	6	\$5.40 (1000)
200	1000	—	3.1 50	1	6	\$14.50
200	1000	—	2.8 90	1	6	\$28.00
200	1000	—	3.8 200	1	6	\$64.00
200	1000	—	2.8 300	1	8	\$99.00
400	600	1000, 1200	2.84 251	30	8	\$290 (1 to 9)
—	1500	—	<3.4 2.5	—	<0.7	POR*
—	1000	—	<2.0 10	—	<0.85	POR*
—	1000	—	<2.2 20	—	<1.3	POR*
200	600	15	2.4 300	10	16	POR*
200	600	15	2.4 400	10	16	POR*
200	600	15	2.4 700	10	16	POR*
200	600	15	2.4 800	10	16	POR*

SURGE (NONREPETITIVE) ON-STATE CURRENT	CRITICAL RATE OF RISE OF ON-STATE CURRENT	CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE	REPETITIVE PEAK REVERSE VOLTAGE	ON-STATE VOLTAGE	GATE-CONTROLLED TURN-OFF TIME	PRICE (1000)
I_{TSM} (A)	di/dt (A/ μ SEC)	dV/dt (V/ μ SEC)	V_{RRM} (V)	V_{TM} AT I_{TM} (V) (A)	t_{GQ} (MAX) μ SEC	
125	200	1000	13*	3.45 50	6	CIRCUIT A ~\$35, B ~\$40, D ~\$35
270	200	1000	13*	3.1 90	6	CIRCUIT A ~\$65, B ~\$75, D ~\$60
440	200	1000	13*	3.1 150	6	CIRCUIT B ~\$140
450	500	1000	—	— —	5.1	POR** (AVAILABLE 4TH QTR '85)
400	200	1000	—	3.6 100	8	~ \$150
400	250	1000	—	3.5 150	7	~ \$200
400	200	1000	—	4.5 100	8	~ \$80
500	200	1000	—	4.3 200	10	~ \$145
550	200	1000	—	2.0 50	8	V_{DRM} 1200 ~\$61, 1300 ~\$67
880	200	1000	—	2.2 100	8	V_{DRM} 1200 ~\$98, 1300 ~\$109
1540	50	300	—	2.2 200	8	V_{DRM} 1200 ~\$136, 1300 ~\$151
400	200	1000	15*	3.6 200	8	CIRCUIT B ~\$75
500	200	1000	15*	3.8 200	10	CIRCUIT B ~\$150



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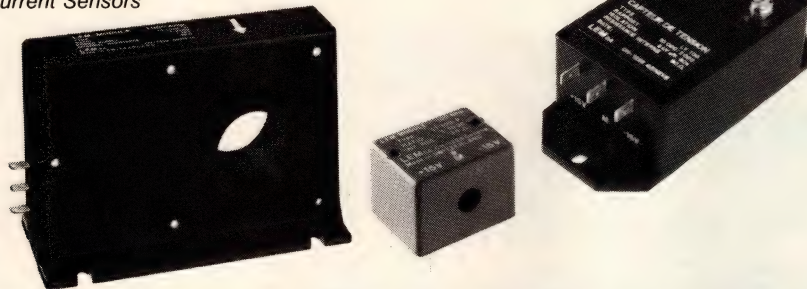


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CIRCLE NO 40

TECHNOLOGY

tors, will introduce a 2500V, 1700A GTO thyristor in late 1985. Its target specs include 1000V/ μsec critical dV/dt, 150A/ μsec critical dI/dt, and a gate-turn-off gain of about 5 to 7. The company plans to follow this with 4500V GTO thyristors, beginning with current ratings of 3000A and working downwards to 200A devices.

Expect the addition of 160 and 400A power modules to BBC Brown Boveri's 90A version, and watch for power modules and pressure packs from another West German company, Semikron, which expects to enter the market in 1986 with devices rated between 100 and 250A. In the UK, 1986 should also see the first GTO-thyristor products from Westcode Semiconductors.

Although GTO thyristors are replacing SCRs in all but the highest power applications, in a few years they may themselves face replacement by another device currently under development. The static-induction thyristor (SIT), also known as the field-controlled thyristor, promises straightforward voltage control of its gate, low on-state voltage, and operation at very high frequencies.

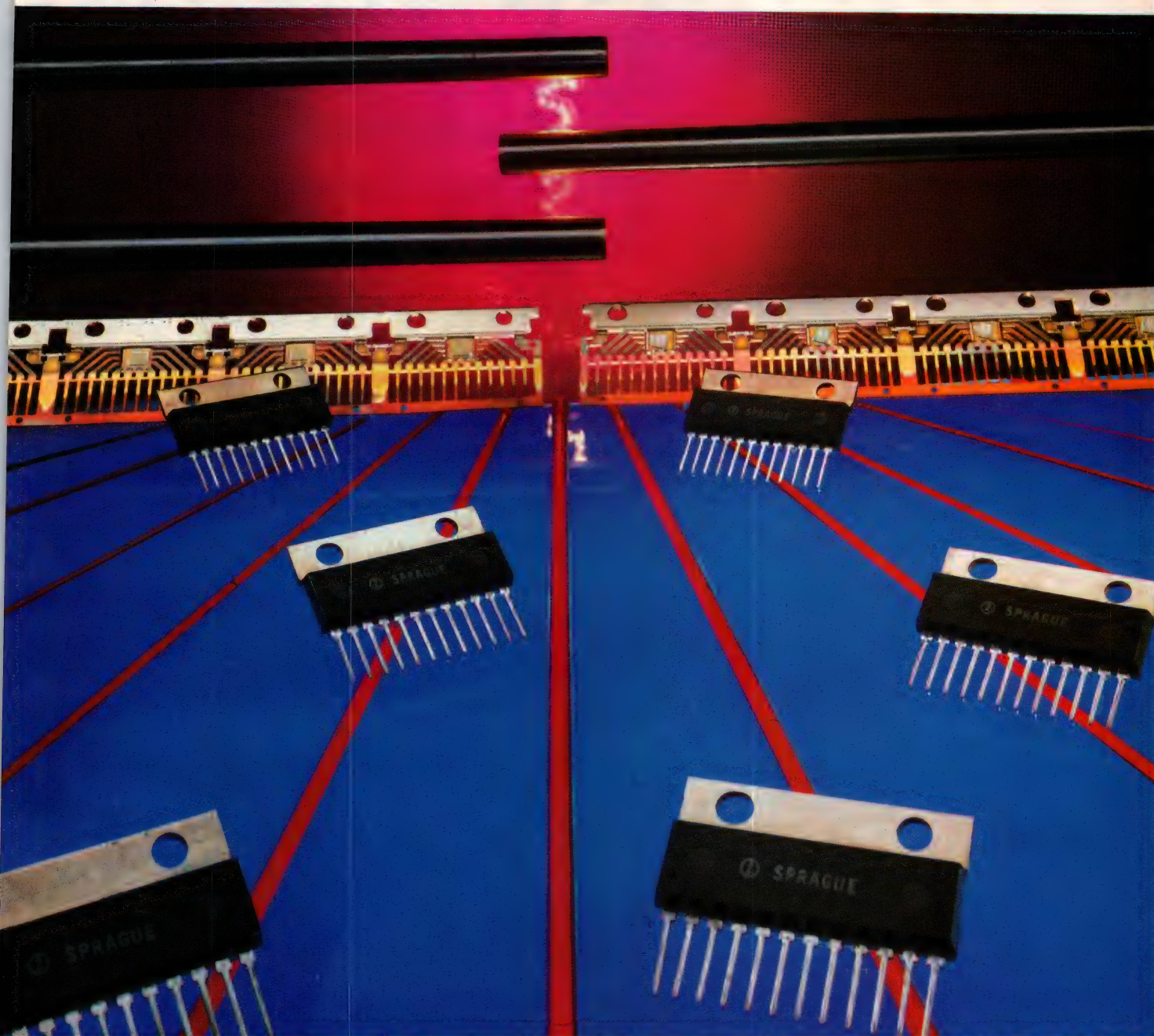
The SIT requires the processing of a large wafer area with very fine horizontal geometries and deep vertical-diffusion zones, and so fabrication techniques are not yet available to make the device commercially procurable. Dr Paul Taylor, head of power-device design at Marconi Electronic Devices Ltd, believes that SITs will eventually match the voltage capabilities and probably exceed the current capabilities of current GTO thyristors, yet operate at switching frequencies as high as 100 kHz. In his estimation, though, commercial devices could be at least five years away.

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CIRCLE NO 43

TECHNOLOGY UPDATE

Multiple-access fiber-optic couplers enhance data-link performance

Tom Ormond, *Senior Editor*

Multiport fiber-optic couplers (devices with three or more access points) can add flexibility and sophistication to your fiber-optic system and network designs: They allow for bidirectional transmissions; let you tap, split, and combine transmissions; and permit you to multiplex signals.

Fiber-optic couplers, once mere laboratory curiosities, are now available off the shelf. They're affordable, too, considering the system enhancements they provide. Naturally, because no one coupler can provide all the aforementioned

capabilities, vendors offer couplers in a wide range of configurations and coupling technologies (see **box**, "The technology of fiber-optic couplers").

Interfacing multiple locations

AMP, for example, offers six splitters/combiners—three squid types and three unitized types. Squid models come in 1×2-, 1×3-, and 1×7-port versions. Fiber-cable legs are individually terminated on one end of the assemblies; fibers on the other end are clustered into a bundle that's terminated with a single Optimate simplex connector.

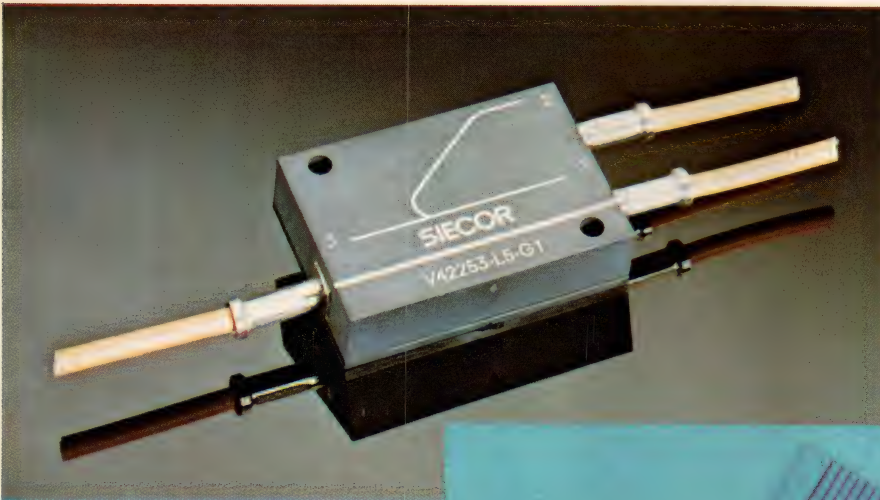
AMP's unitized devices are avail-

able in 1×7- (140- μ m fiber), 1×7- (250- μ m fiber), and 7×1×7-port star configurations. The devices are housed in a thermoplastic material that's fitted with metal Optimate simplex connectors.

Insertion loss for these splitters/combiners depends on your particular interface. When you design them into a system employing a 400- to 500- μ m source and a detector with a 400- μ m active window, the devices can transmit over distances of as great as 1 km and operate over -20 to +60°C.

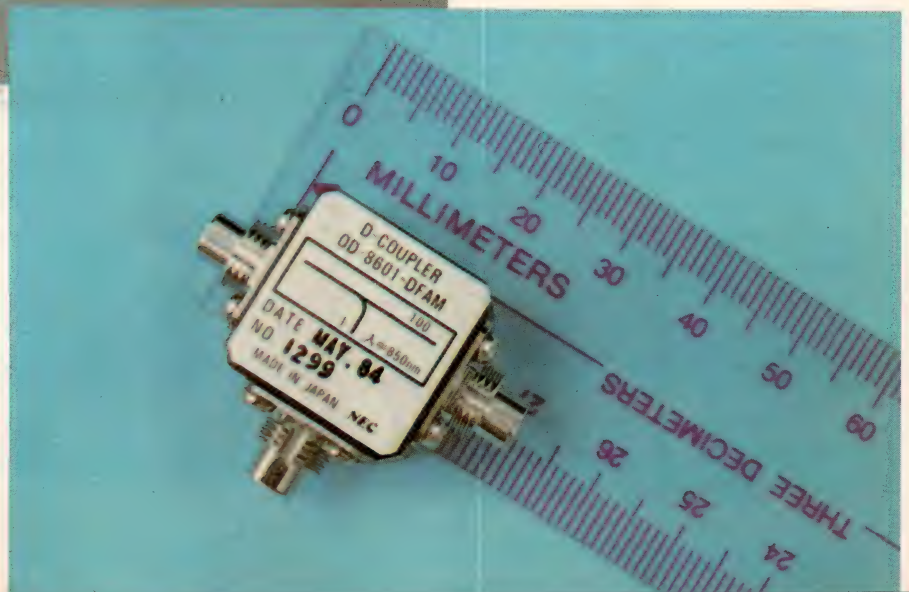
NEC offers similar splitters/combiners: The OD-8601 optical directional coupler has three ports; the OD-8602 has four. Both devices offer three splitting ratios—1:1 (K), 10:1 (L), and 100:1 (M). Standard versions of both devices work with either 50- μ m-core, graded-index fiber or 80- μ m-core, step-index fiber.

Both couplers accommodate transmission in the short (850 nm) or long (1300 nm) wavelength regions. Maximum insertion loss specs at 2 dB (1.5 dB typ). Minimum isolation measures 15, 20, and 30 dB



Performing multiplexing and demultiplexing, the wavelength-division couplers from Siecor feature insertion loss of less than 1 dB and are available in pigtail or connector versions.

Available in 3- or 4-port designs, the directional couplers from NEC Electronics offer splitting ratios of 1:1, 10:1, and 100:1. They are compatible with both step- and graded-index fibers and are housed in a 20×16×20-mm package.



for K, L, and M versions, respectively. Splitting-ratio accuracy specs at ± 1 , ± 2 , and ± 3 dB.

Couplers are also available for single-mode fiber. Canstar provides its SM line of couplers in any configuration ranging to four input and four output ports. Designed for test equipment, telemetry, sensor, and telecommunication applications, the couplers can operate at 850 or 1300 nm, depending on the model.

Three of the Canstar models have splitting ratios of 1:1 (SM3C), 1:1

(SM4C), and 4:1 (SMS4 $\times$ 4). Maximum insertion loss specs at 1, 1, and 1.5 dB, respectively, and directivity is greater than 45 dB for all models. Maximum thermal, polarization, and wavelength coefficients are 0.002 dB/ $^{\circ}$ C, ± 0.1 dB/360 $^{\circ}$, and 0.03 dB/nm, respectively.

The 850-nm fibers have a 0.1 numerical aperture (NA), a 4.5- μ m core, and a 770-nm cutoff wavelength. The 1300-nm fibers have a 0.1 NA, a 10- μ m core, and a 1250-nm cutoff wavelength. The couplers

are supplied with fiber pigtailed and operate over -50 to $+70^{\circ}$ C.

Employing fused-fiber technology, TS Series transmissive star couplers from Phalo evenly split or combine energy between the input and output ports for optical data collection or distribution. They are available with 0.5m-long cabled or buffered graded- or step-index fiber leads (50- or 100- μ m core). Input and output port count can be as high as 32 $\times$ 32; standard couplers are available in 8 $\times$ 8-, 16 $\times$ 16-, and

The technology of fiber-optic couplers

Taps, splitters, and combiners are the simplest forms of single-wavelength fiber-optic couplers. A tap (or T-type coupler) is a 3-port device that divides a transmitted optical signal into two channels. Taps typically remove only a small portion of the main signal; you'd use them mainly in applications requiring feedback control of the optical power, or in applications in which you want to provide a signal-monitoring capability.

Splitters take an optical signal and divide it into several channels; combiners are simply splitters configured in the opposite direction. Unlike taps, splitters divide the signal equally among the output fibers. Typically, you'd use splitters in data-link applications in which a significant portion of the main transmitted signal must be channeled to peripheral devices.

In T-type couplers, the tap ratio defines the fraction of light energy that's coupled at each access point in a link. Tap ratio is a critical system variable in a data bus. Another critical variable is excess loss, the energy lost in the coupler because of reflection and absorption. The sum of the excess loss and the power-splitting loss (a function of the tap ratio) is the coupler insertion loss at each terminal in the network.

T-type couplers employ several different techniques. One kind of T coupler contains a combination of lenses and a beam splitter. As the light leaves one fiber, a lens collimates it. When the light hits the beam splitter, the beam splitter directs the light to other lenses, which then refocus the light onto the appropriate output fibers. You can use this approach with step- and graded-index fibers.

Some T-type couplers employ a mixing-rod concept, in which the incoming fiber is fastened to one

end of a thick glass rod, and the output fibers are attached to the other end of the rod. As light enters the rod, it bounces around randomly and then exits to the output fibers. You can use this technique only with step-index fibers.

A third type of T coupler employs identical fibers and fuses them into a biconical taper. You can also use this biconical-taper-based coupler to fabricate power combiners and duplex couplers by fusing two or more fibers of different diameters.

Because of insertion-loss buildup, T couplers aren't practical for use in systems with many access points. Instead, you can use star couplers—devices that have M number of ports on one side and N number of ports on the other side. To qualify as a star coupler, N must be greater than two; M can be between one and N. Stock couplers typically have values for N of 4, 8, 16, 32, and 64.

Star couplers come in two varieties: transmissive and reflective. The transmissive star coupler's input ports are essentially isolated from each other; the reflective star's ports are coupled. Both types of star couplers are composed of input fibers, output fibers, and a mixing region, which is usually either a glass rod, a reflecting mirror and lens, or a fused, tapered zone.

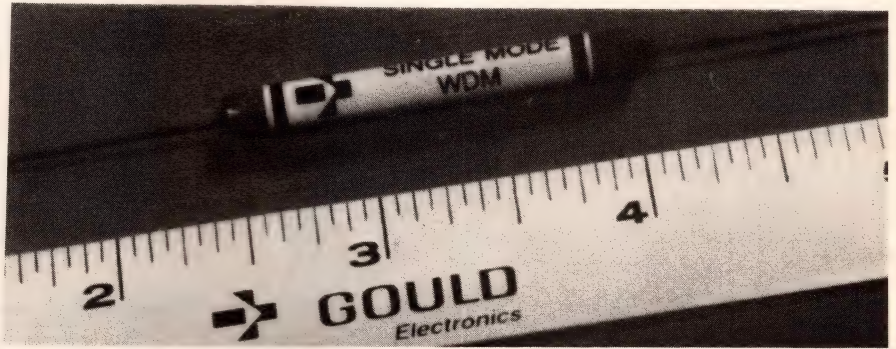
Multiport transmissive star couplers that use a fused, tapered zone for a mixing region are manufactured by cutting the desired number of fibers and twisting them together into a hexagonal bundle or other densely packed formation. The fibers are then put under tension and placed over a controlled heat source. As the fibers soften, the claddings fuse and the tension pulls the fibers into biconical tapers with a central fused section. By varying the applied tension, the flame temperature, and the applied torsion, the manufacturer can

TECHNOLOGY UPDATE

20×20-port designs.

The TS Series couplers feature maximum insertion loss ranging from 2 to 3 dB. Maximum port-to-port throughput factor is -11 to -15.5 dB, and typical directivity measures >-40 dB. Operating range spans -50 to +85°C.

For multiplexing and demultiplexing in local-area networks, for 2-way video/data links on a single fiber, and in long-haul data transmission links, you can use Gould's 2×2-port single-mode, wavelength-



Employing fused-fiber technology, Gould's 2-channel wavelength-division-multiplexing (WDM) couplers operate with 1300- and 1550-nm wavelengths. They feature an excess loss of <0.5 dB and a wavelength isolation of -16 dB min.

closely control the diameter, shape, and length of the fused section.

Whatever the fabrication technique, the reflective star coupler is generally more versatile than the transmissive star. Even after the reflective star has been constructed, you can select or vary its relative number of input and output ports. In the transmissive star, the number of input and output ports is fixed during the initial design and fabrication.

Despite its versatility, the reflective star is usually less efficient than the transmissive star, because a portion of the light fed into the reflective star is injected back into the input fibers. A transmissive star is twice as efficient as a reflective star that has the same number of input and output ports.

Because reflective and transmissive star couplers have their own particular advantages and disadvantages, your network topology is the most important factor that you must consider when choosing a star coupler for your application.

Boosting your system performance

If you're designing fiber-optic data links, you'll find wavelength-division-multiplexing (WDM) couplers very useful. Such couplers can, for example, increase the effective bandwidth of your system. They allow you to develop 2-way communications over a single fiber, and, because they allow your system to operate at the longer wavelengths, they provide a simple means of upgrading an existing system.

Manufacturers use several different technologies to make WDM couplers. One method, the fiber-fusion technique, lends itself well to wavelength-division multiplexing—it's a simple matter to fuse

fibers optimized for a wide range of wavelengths. Two other methods employ miniature optical components: the graded-index (Grin) lens, and the spherical retroreflecting mirror.

In the Grin-lens coupler, light from the transmitting fiber strikes a dividing or combining element (a beam splitter or dichroic mirror) and then strikes the Grin lens. The Grin lens refocuses the collimated light onto another fiber or fibers. Because the beam has been collimated, the dichroic mirrors can handle the closely spaced optical wavelengths.

The Grin-lens coupler is harder to make than are other optical components; it doesn't lend itself to large-scale automatic manufacturing techniques. To focus a Grin lens, the manufacturer must perform active alignment of the fibers. When light exits the transmitting fiber, the manufacturer monitors the receiving fiber for coupled power. The manufacturer positions the receiving fiber for peak power and then fastens the fibers in place.

Unlike the Grin-lens coupler, the retro-reflecting-mirror coupler design relies on the fact that light exiting from the center of curvature of a spherical mirror is reflected perfectly back onto itself. The mirror has no geometric aberrations and no chromatic aberrations.

A typical dual-wavelength, retroreflective coupler has two spherical surfaces—one with a dichroic mirror coating and the other with a metallized mirror coating. The dichroic coating transmits the source output, and the second mirror reflects the source output to the link fiber. The dichroic mirror then reflects the link fiber's output to the detector port's fiber.

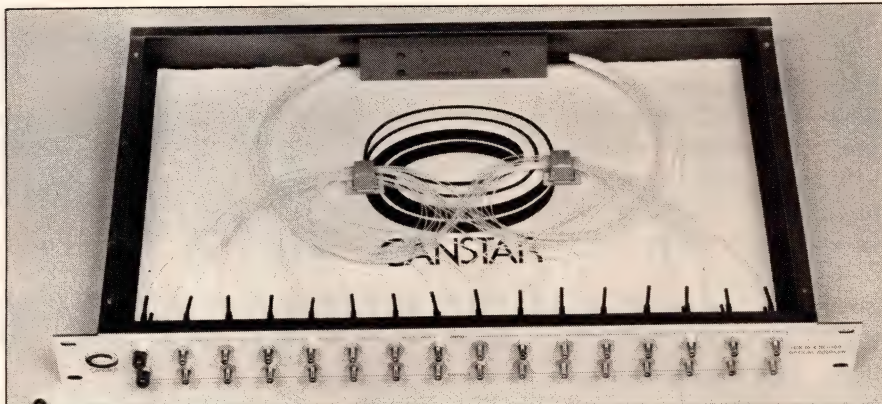
TECHNOLOGY UPDATE

dependent couplers. The devices are fabricated with fusion technology and come in very small packages (4×0.4 cm).

These WDM (wavelength-division-multiplexing) couplers operate with 1300- and 1550-nm wavelengths. Maximum excess loss is 0.5 dB, and wavelength isolation is -16 dB min. Maximum thermal and polarization coefficients spec at $\pm 1.5\%$ and $\pm 1\%$, respectively. The units are supplied with 1m-long fiber pig-tails, and they operate over -55 to $+125^\circ\text{C}$.

American Photonics, Kaptron, and Siecor all offer WDM couplers that utilize optical-component technology. The WC4200 Series couplers from American Photonics use Grin (graded-index) lens techniques. Available for multiplexing (M suffix) and demultiplexing (D suffix), the devices are designed for 2-channel WDM transmission and can be used in either unidirectional or bidirectional systems.

The WC4200 Series includes devices whose operating wavelengths range from 780 to 1600 nm. You can select models that pair short or long wavelengths or models that offer a combination of short and long wavelengths. Typical port-to-port insertion-loss figures range from 1.5 to 2 dB max, and minimum port-to-port



Completely enclosed for maximum protection, Canstar's star couplers come in transmissive and reflective designs. Compatible with stand-alone or rack-mounting operation, they are available with port counts ranging to 64×64 , and can operate with both step- and graded-index fiber.

optical isolation measures from 18 to 50 dB. The couplers employ 50- μm -core fiber with a 0.2 NA, are housed in a package measuring $13 \times 13 \times 63$ mm, and operate over -50 to $+65^\circ\text{C}$.

Kaptron also takes a dedicated-service approach, offering devices specifically designed for multiplexing (WDM-01) and demultiplexing (WDM-02) tasks. The devices are housed in a package ($7/16 \times 2 1/2$ in.) that lends itself to pc-board mounting. Both devices are dual-channel couplers; different models are available for operation at the following wavelengths: 820/1300, 1200/1300, and 1300/1520 nm.

The WDM-01 and WDM-02 both

employ mirrors with low-loss dichroic coatings; the mirrors let you multiplex (WDM-01) and demultiplex (WDM-02) wavelengths that are separated by as little as 7%. The couplers use high-quality reflective optics, which improves imaging (less aberration) and increases immunity to radiation-induced loss. Insertion loss measures 1.5 dB max, and crosstalk doesn't exceed -30 dB. The devices operate over -40 to $+50^\circ\text{C}$.

Siecor's WDM coupler serves as an optical multiplexer and demultiplexer. Available with pigtailed (500 mm long) or with SMA or DIN connectors, the coupler operates with two optical channels and has one signal in each of the following wavelength windows: $\lambda_1 = 1150$ to 1600 nm, and $\lambda_2 = 800$ to 900 nm.

The WDM coupler is available with two types of fiber: 50- μm -core fiber with a 0.2 NA, and 100- μm -core fiber with a 0.29 NA. The device is fabricated with interference-filter technology, which results in insertion loss of <1 dB for pigtail versions and <2.5 dB for connector versions. With or without the connectors, the couplers' crosstalk is at least -20 dB, and the operating temperature spans -10 to $+55^\circ\text{C}$.

EDN

For more information . . .

For more information on the fiber-optic couplers discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

American Photonics Inc
71 Commerce Dr
Brookfield Center, CT 06805
(203) 775-8950
Circle No 718

AMP Inc
Eisenhower Blvd
Harrisburg, PA 17105
(717) 564-0100
Circle No 719

Canstar Communications
1240 Ellesmere Rd
Scarborough, Ontario
Canada M1P 2X4
(416) 293-9722
Circle No 720

Gould Inc
Defense Electronics Div
6711 Baymeadow Dr
Glen Burnie, MD 21061
(301) 760-3100
Circle No 721

Kaptron Inc
3460 W Bayshore
Palo Alto, CA 94303
(415) 499-8008
Circle No 722

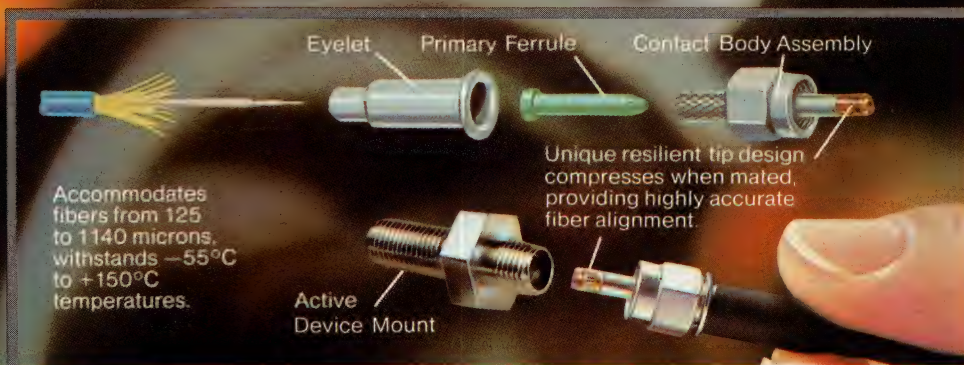
NEC Electronics Inc
401 Ellis St
Mountain View, CA 94043
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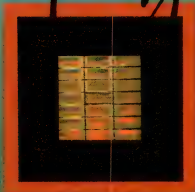
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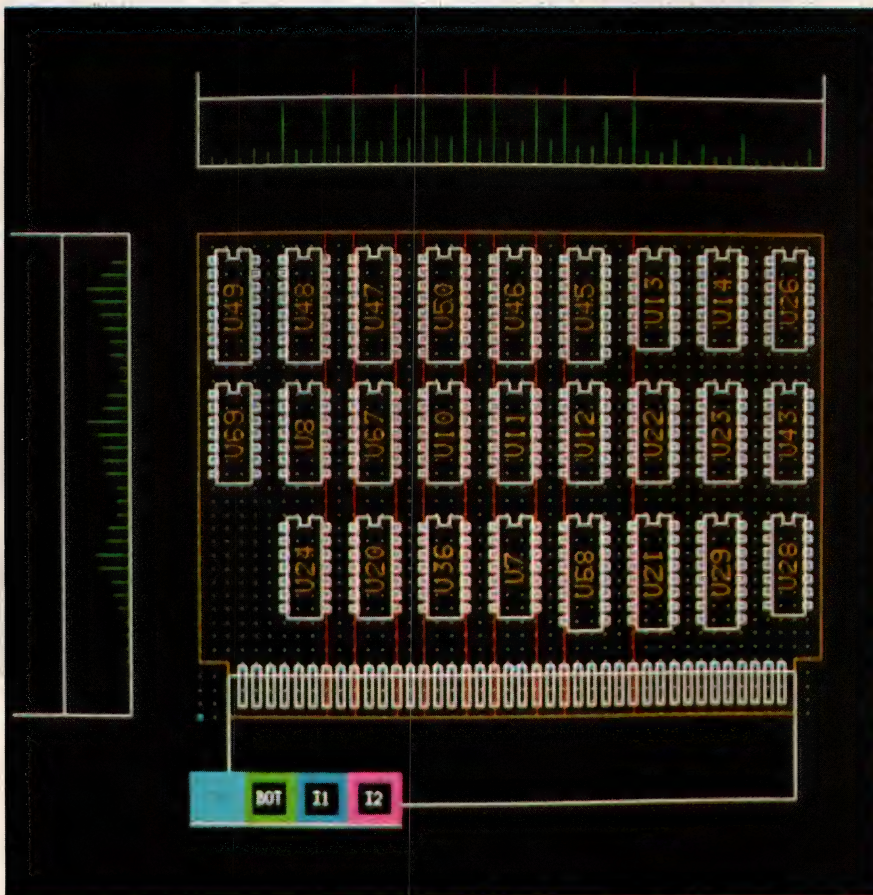


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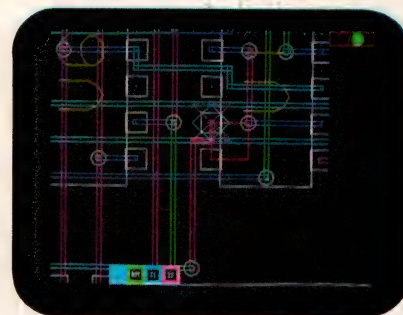
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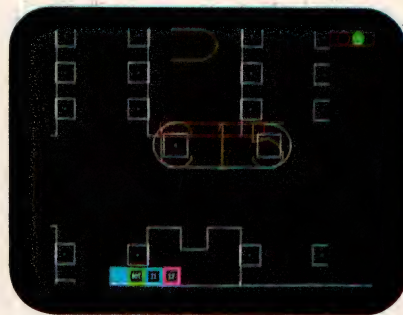
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IBM PC-compatible single-board controller runs tape, floppy, and Winchester drives

The Universal Mass Storage Controller promises to relieve the expansion-slot constraints of the IBM PC and compatible devices. The single-board, single-slot controller, compatible with the IBM PC and PC/AT, includes interfaces for tape drives as well as floppy- and Winchester-disk drives. The board sports improved data-transfer rates over competitive products, thus increasing its value in Unix-like environments.

The unit's tape interface meets the Quarter Inch Committee's QIC-36 specification; this spec requires virtually no intelligence on the part of the tape drive, so you can use a low-cost model. The board also provides an SA-450-compatible floppy-disk interface that can handle four drives.

The unit's Winchester controller, however, provides the most significant performance improvements. Although most IBM PC controllers use a Modified Frequency Modula-

tion (MFM) encoding scheme for hard disks, the Universal Controller offers MFM capabilities or the firm's proprietary Run Length Limited (RLL) encoding. An IBM PC-compatible hard disk can function with either scheme, but the RLL method provides such advantages as increased capacity and improved data-transfer rate.

For example, a typical hard disk that can hold 60M bytes of MFM-encoded data will actually store 92M bytes when it's formatted with RLL encoding. The capacity increase requires no change to the disk drive. In addition, the board increases the normal 5M-bps data-transfer rate to 7.5M bps. These performance enhancements are due in part to the board's ability to use one-to-one interleaving on the disk drive.

A CMOS chip set provides most of the controller board's capabilities. The DC1001 controller chip includes a data serializer/deserializer, encoding/decoding logic, error-checking

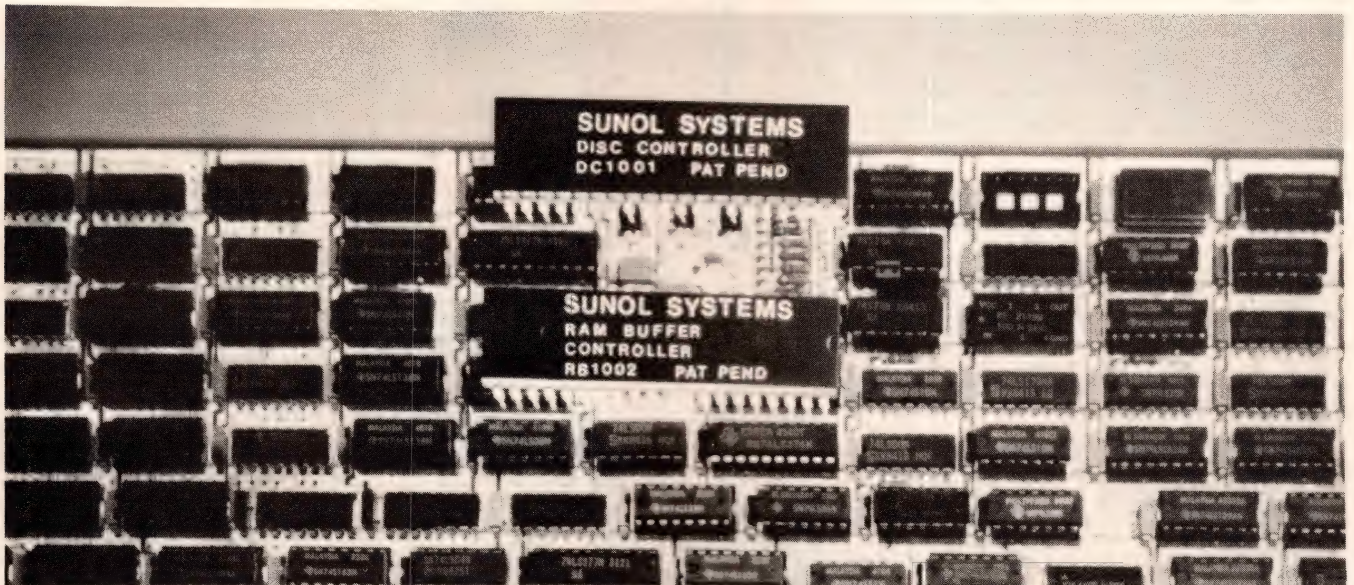
and -correcting logic, and interface/glue logic. In addition, the chip contains registers to store parameters for each of the peripherals.

The controller chip ties to the second chip in the set, an RB1002 RAM buffer, through one of the buffer's three DMA channels. The RAM buffer also includes a host interface port and a dynamic-RAM controller. The chip set supports data-transfer rates to 15M bps.

In addition to the chip set, the Universal Mass Storage Controller includes an onboard μ P and 16k to 64k bytes of RAM. The board also allows transparent communication between the tape and disk drives. The firm plans deliveries in June and expects the board to sell for \$595.—**Maury Wright**

Sunol Systems, 1187 Quarry Lane, Pleasanton, CA 94566. Phone (415) 484-3322.

Circle No 726



The 7.5M-bps data-transfer rate and increased Winchester capacity—the result of RLL encoding—allow the Universal Mass Storage Controller to increase IBM PC and PC/AT system performance using only one expansion slot.

Thick-film data-acquisition hybrid IC combines T/H amp, programmable-gain stages

Model AD365, a complete hybrid data-acquisition front end for A/D converters, provides wide dynamic range for the processing of analog signals. It incorporates a programmable-gain amplifier (PGA) and a track/hold (T/H) amplifier on a ceramic substrate. The PGA chip, the manufacturer's AD625, offers gains of 1, 10, 100, and 500; you program the gains with a 2-bit digital word. In addition, the hybrid incorporates the manufacturer's AD7502 CMOS multiplexer for switching the gains of the PGA.

The PGA's gain inaccuracy is 0.05% max for gains from 1 to 100 and 0.1% max for a gain of 500. Nonlinearity limits are one-tenth the gain-inaccuracy figures. Gain-drift figures for the cited gain ranges are 5 and 10 ppm/°C, respectively. Input offset voltage is 200 μ V max; offset drift is 2 μ V/°C max.

The PGA has a fully differential, instrumentation-style input stage and a guard terminal that lets you, for example, bootstrap the capacitance of an input cable. Input impedance is typically 1 G Ω in parallel with 5 pF. The noise at the input is 0.2 μ V p-p typ over the 0.1- to 10-Hz range.

The PGA's output settles within a 0.01% error band in 10 μ sec max for gains of 1 and 10 and in 15 and 50 μ sec max for gains of 100 and 500, respectively. Small-signal bandwidth, for the four gain values in ascending order, is typically 800, 400, 150, and 40 kHz.

The internal T/H amplifier uses the manufacturer's AD585 chip. The T/H amplifier contains a 100-pF hold capacitor—this value, in conjunction with the amplifier's input bias, yields a 1V/sec max droop spec, a figure that doubles every

10°C. The amplifier specs an open-loop gain of 100,000 min and 0.01% max nonlinearity: The latter figure makes the T/H amplifier suitable for 12-bit applications.

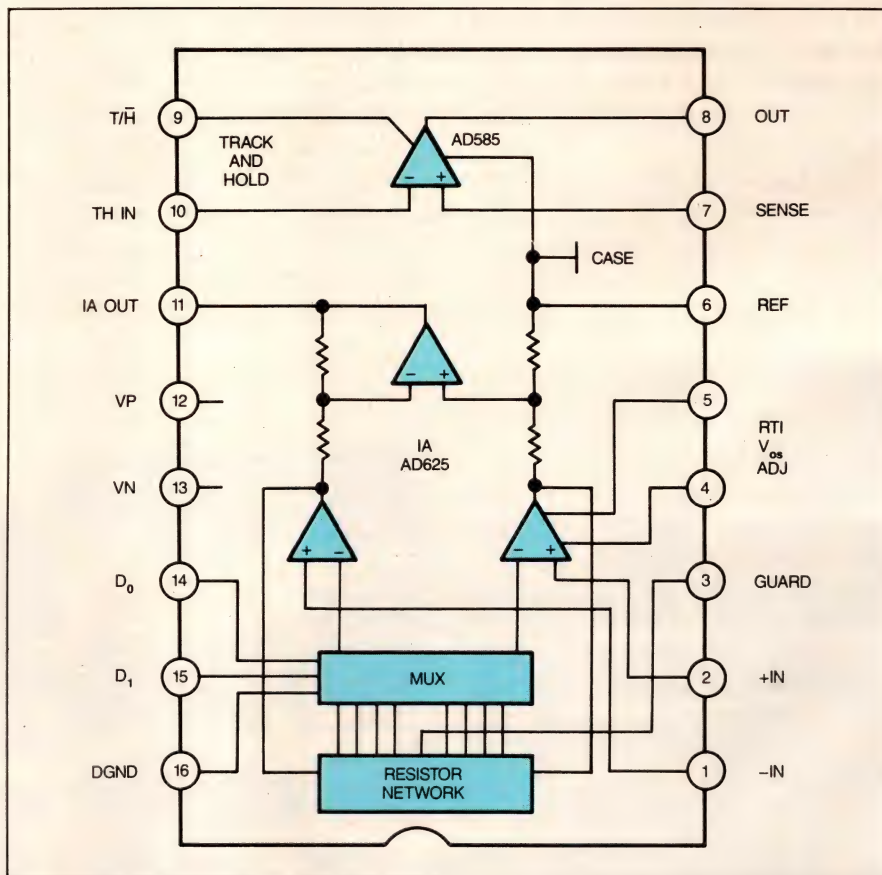
The 0.5-nsec typ aperture uncertainty (or jitter) allows sampling of signals with frequencies as high as 77.7 kHz (for $\frac{1}{2}$ -LSB max error) in 12-bit systems. The data sheet gives diagrams for two 12-bit A/D-conversion systems—one uses an AD578 A/D converter and yields 117.6-kHz throughput; the other uses an AD574 converter for 26.3-kHz throughput. According to Nyquist's

theorem, of course, the frequency of the sampled signal is limited to half these throughput figures.

The AD365 is housed in a 16-pin, metal single-width DIP. The hybrid dissipates 550 mW max and operates over -25 to +85°C. Its gain-selection and T/H digital inputs are TTL and CMOS compatible. The circuit operates from 4.75 to 17V and -11 to -17V supplies. \$61.95 (100).—**Bill Travis**

Analog Devices Inc., Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 730



A complete front end for a data-acquisition system, Model AD365 from Analog Devices incorporates the company's monolithic programmable-gain amplifier and track/hold amplifier in a thick-film hybrid circuit. All the hybrid's accuracy and nonlinearity specs render the device suitable for use in 12-bit analog-input systems.



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Low-power RS-232C and -423 line-driver IC operates from wide power-supply range

An RS-232C and -423 quad line driver (**Fig 1a**) works from power supplies ranging from ± 5 to ± 15 V, vs the ± 9 to ± 15 V required by the earlier, industry-standard 1488 driver. Moreover, the LT1032 consumes 1-mA max supply current vs the 1488's 34 mA max.

The device features both current and thermal limiting on the outputs for protection against externally applied voltages as high as ± 30 V. The outputs have low saturation drops: 0.3V max in the high state and 0.9V max in the low state (with 2-mA output) vs the 1488's drops of approximately 3V. **Fig 1b** shows a typical device's saturation drops vs output current.

An on-off control allows you to

shut off the IC completely—when off, the device consumes no supply current. The LT1032 also includes a strobe pin that you can use to force all outputs low, independently of the IC's input conditions or the on-off terminal's state. The strobe line needs 3V min at 2 mA to perform its role.

Another useful control pin is the response terminal. It allows you to vary the device's nominal 15V/ μ sec slew rate by $\pm 50\%$. To use the response trim, you inject current into the response terminal—50 μ A increases the slew rate by 50%; -50 μ A reduces it by the same amount.

The LT1032's TTL-compatible inputs source 2 μ A typ to the IC's driver in the high state, 10 μ A typ

in the low state. By contrast, a 1488 sources 1.6 mA max in the low state. Like the 1488, the LT1032 sinks or sources at least 10 mA at its outputs. The outputs assume a high-impedance (open) state when the device is off or powered down.

Packaged in a 14-pin plastic or ceramic DIP, the LT1032 is available in commercial (0 to 70°C) or military (-55 to +125°C) versions. The commercial LT1032CN costs \$2.95 (100); the MIL-STD-883C LT1032MJ, \$10.95. —**Bill Travis**

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 942-0810.

Circle No 731

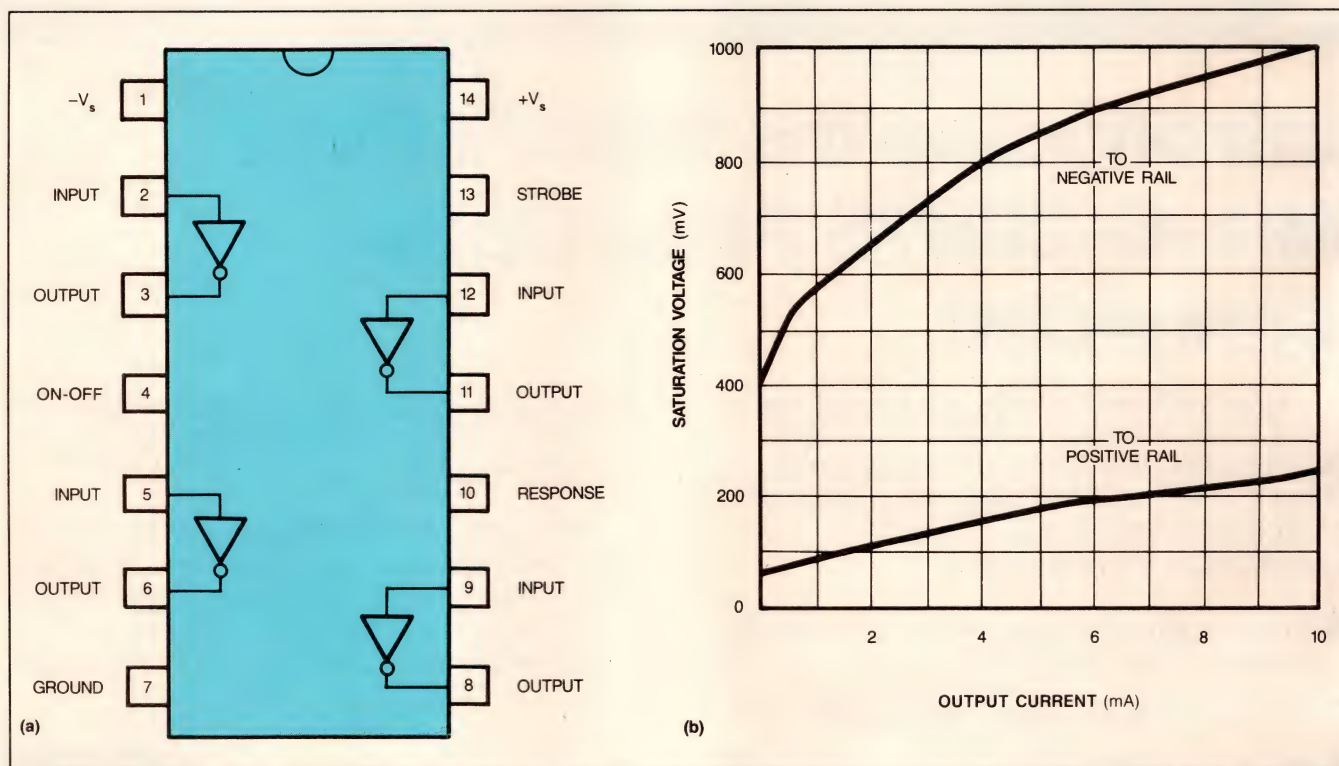


Fig 1—Low saturation drops allow a wide supply range for Linear Technology Corp's LT1032 RS-232C and -423 line driver (**a**). For example, at 2-mA output current, the saturation drops are approximately 700 and 100 mV (**b**), referred to the negative and positive rails, respectively.

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Library file of devices for CAD systems describes logical and physical specs

The Cache component library describes a wide range of electronic devices in detail. These description files can communicate with CAE and CAD systems to support electronic design.

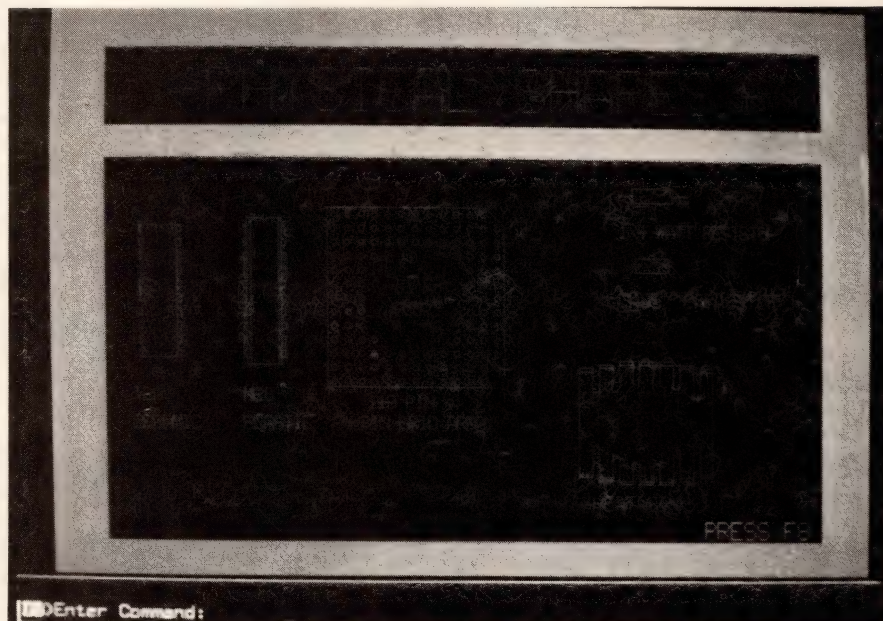
Many design-automation systems don't include complete device libraries. The Cache component library solves this problem by offering files in the Electronic Device Interchange Format (EDIF), a format that is becoming a standard for CAE/CAD software.

To serve both logical- and physical-design needs, the library supports schematic capture and mask layout. Logic files contain at most two hierarchical levels. Physical representations of chips give shapes and pin layouts.

A typical device file requires 7k bytes of memory. Each device file comprises a pin I/O listing, a logic description, timing and electrical characteristics, maximum and minimum ratings, and operating conditions.

The information in the component library comes from data sheets published by various suppliers of electronic parts. When these suppliers issue changes to their data sheets, the developers of the device library will release updates within 60 days.

The device library contains schematic device representations, logic diagrams, outline drawings, and parametric data for 5000 standard ICs. The initial version of the device library furnishes software models of 1800 TTL ICs from data sheets supplied by Texas Instruments (Dallas, TX), National Semiconductor (Santa Clara, CA), and Signetics (Sunnyvale, CA). In addition to TTL devices, the library includes 300 CMOS ICs, from National Semi-



Physical shapes supplied by the Cache component library include all standard IC packages, passive elements, and mechanical parts.

conductor and Texas Instruments, and 200 ECL ICs, from Motorola (Phoenix, AZ) and Signetics.

Files in this library also offer memory ICs, μ Ps and μ P support chips, and linear devices. Vendors of these supplementary ICs include Mostek (Carrollton, TX), Motorola, Intel (Santa Clara, CA), Advanced Micro Devices (Sunnyvale, CA), RCA (Somerville, NJ), and National Semiconductor.

Besides ICs, the library files include discrete and power semiconductors, optoelectronic devices, resistors, and capacitors. Some of the sources of these devices are RCA, Texas Instruments, Motorola, Hewlett-Packard, General Instrument (Palo Alto, CA), Allen-Bradley (Milwaukee, WI), and Sprague (North Adams, MA). Because pc boards generally contain mechanical parts as well as electrical components, the Cache library also offers

files describing a number of mechanical elements, such as switches.

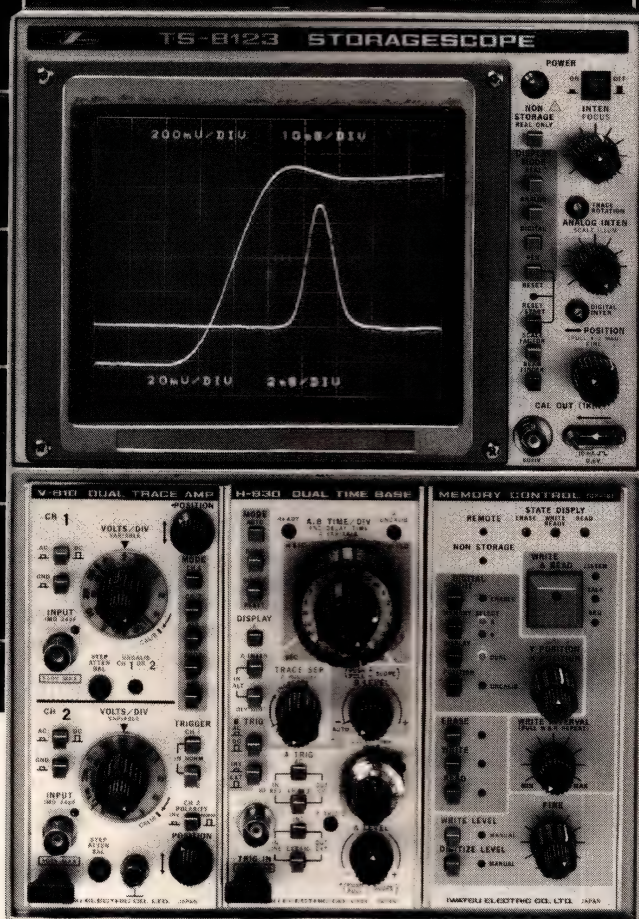
Prices for the Cache library depend on the number of devices you select. Files of typical length cost about \$3000.—*Eva Freeman*

Inacom International, 4380 S Syracuse St, Denver, CO 80237. Phone (303) 694-4200.

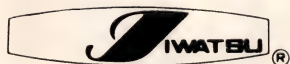
Circle No 729

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The TS-8123 100MHz Storage Oscilloscope incorporates seven major innovations



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3. GP-IB interface for the digital processing of transient phenomena.
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Laser probing system for VLSI designs captures logic states at 20-MHz speeds

The Dataprobe 2010 logic analyzer probes CMOS VLSI chips to verify designs and analyze failures. As the system positions a 1.8- μ m laser spot over the surface of an IC, the logic analyzer captures logic-state diagrams at clock speeds as high as 20 MHz.

The logic analyzer, which uses the solar-cell effect, measures the digital state of an active element inside an IC. The system analyzes these logic states by irradiating a transistor with a 2- μ W laser spot and monitoring the photoelectric response of the transistor. The detector can detect photocurrents in the submicro-ampere range.

If, for example, in a CMOS cir-

cuit, a p-type transistor is in the low state, the laser doesn't produce any current. On the other hand, if the p-type transistor is high, the detector measures a finite photocurrent. Conversely, an n-type transistor generates a photocurrent only when it is at a logical low.

Because only a beam of light interacts with the device under test, this logic-analysis scheme is completely nondestructive. You don't even need to remove passivation layers. Stray magnetic fields probably won't affect measurements, according to the vendor.

The VLSI logic analyzer uses an IBM PC/XT for its main processor. The system can operate either in a

stand-alone configuration or as a satellite of a CAE or CAD host. The interface to design-automation workstations enables the logic analyzer to verify previously simulated signals.

A pipeline processor accelerates measurements. The overall test time per logic node specs at approximately 320 msec, assuming a 1024-state timing diagram, a stage movement of 100 μ m, and a test clock frequency of 10 MHz. Thus, the average test rate is greater than 3 nodes/sec.

A laser-interferometric X-Y stage under computer control positions the probing beam to an accuracy of 1.0 μ m. Because of the accuracy of the stage, the logic analyzer can evaluate devices having design rules as small as 2 μ m.

In addition, the system can test devices having as many as 128 pins. The logic analyzer can handle DIP, flat-pack, pin-grid, and leadless-chip-carrier packages. The system offers 256 analysis channels, each of which may detail from 32 to 1024 states.

The personal computer displays 16 channels at a time. You can scroll displays up or down through all channels, and you can rearrange the order of the channels.

The logic analyzer's internal clock can synthesize frequencies from 200 kHz to 40 MHz, in increments of 100 kHz. If you supply a TTL-compatible external clock, you can operate the system from dc to 20 MHz. \$140,000.—*Eva Freeman*

Mitsui & Co (USA), Semiconductor Systems, 10050 N Wolfe Rd, Building SW2, Cupertino, CA 95014. Phone (408) 725-8797.

Circle No 728



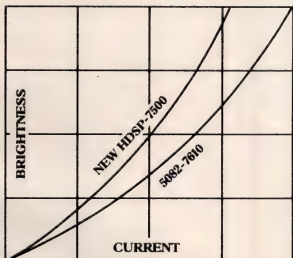
By taking advantage of the solar-cell effect, the Dataprobe 2010 probes logic states of transistors in CMOS ICs without destroying the ICs.

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Drawing digitizer and editor interface with electronic data storage and CAD systems

Model 3000, a drawing-digitizing system, provides an automated link between engineering drawings produced by hand, electronic data-storage systems (which often store drawings in raster form), and CAD systems (which generally use a vector format to store drawings).

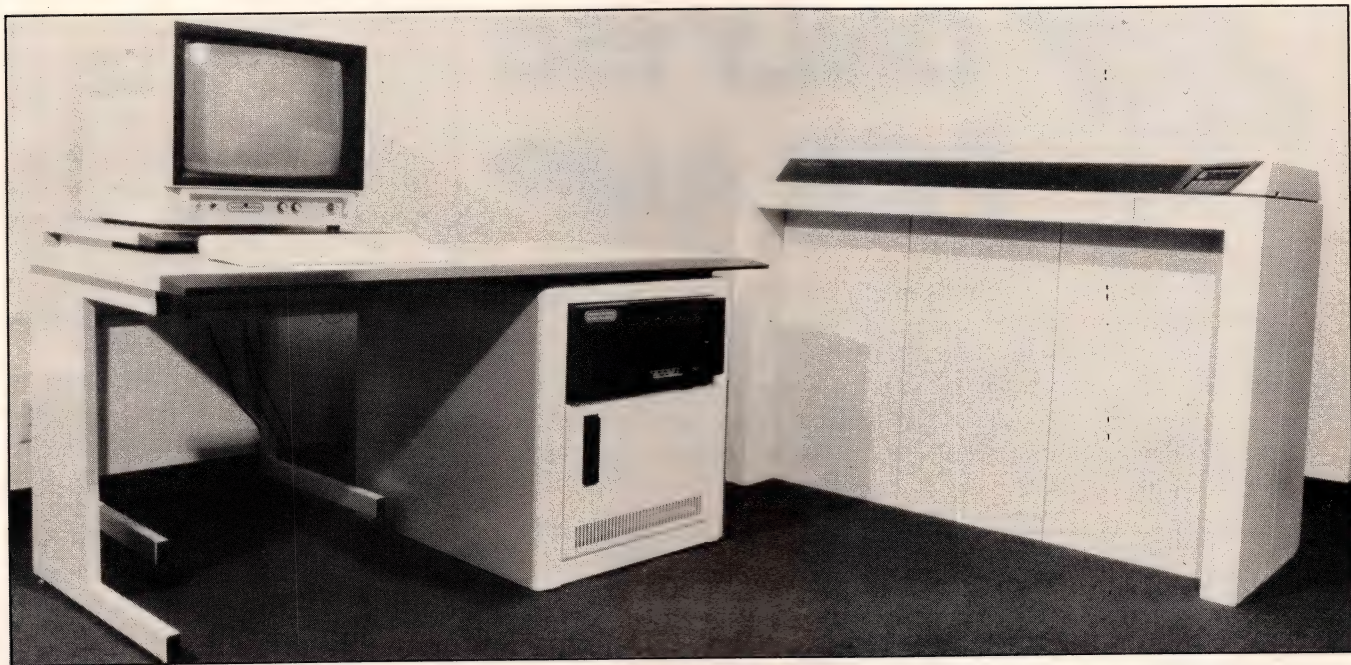
The drawing-digitizer system

looks like a CAD/CAE workstation and includes computer, 19-in. CRT, and mouse. In addition, the system includes a free-standing document scanner connected via a parallel interface. A Versatec-type electrostatic-plotter interface provides hard-copy output capabilities.

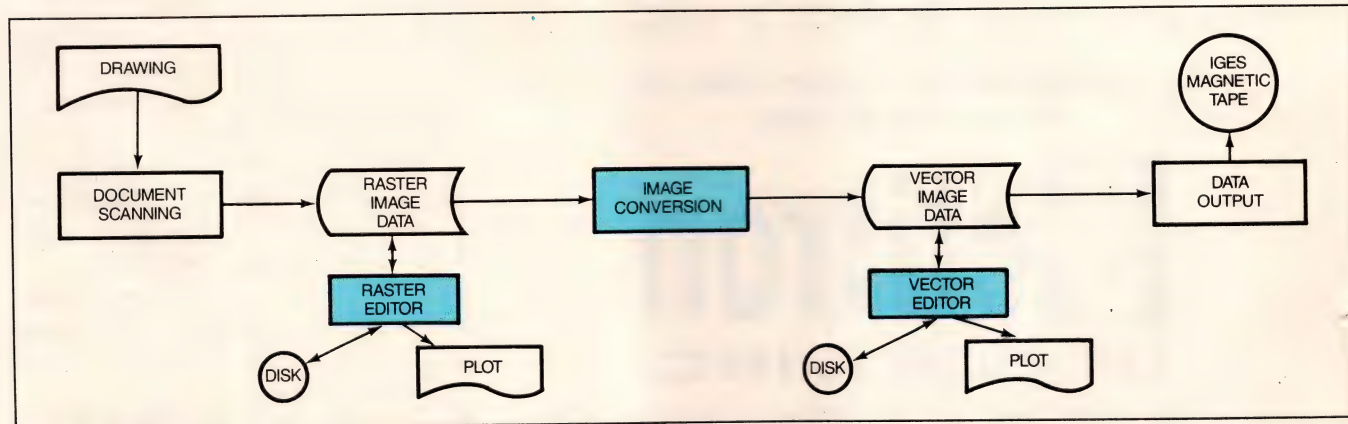
Model 3000 scans an E-size draw-

ing in approximately 90 sec. The system retains the raster image of the document in a dedicated 10M-byte section of RAM. Once the document is stored in memory, the system's software tools become active.

Via the system's raster editor, you can manipulate stored data to clean up a drawing. For example,

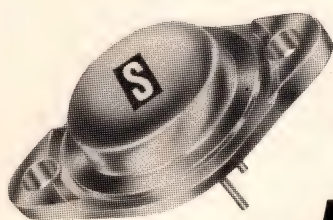


Able to capture, edit, convert, and store drawings, the Model 3000 drawing-digitizing system bridges the gap between various engineering automation tools.



Raster edit, image conversion, and vector edit make up the primary functional blocks of Model 3000's scheme of operation.

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$V_{CE(sat)}$ max	1.25V @ 50A, 5A	2.0 @ 40A, 4A	2.0V @ 30A, 3A
h_{FE} min	10 @ 50A, 5V	10 @ 40A, 5V	10 @ 30A, 10V
f_t min	10 MHz	10 MHz	10 MHz
K Price	\$8.50 ea.	\$7.75 ea.	\$10.50 ea.

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UPDATE

the system includes a speckle-removing feature. To use this feature, you define the size of the speckle you want deleted. The system then searches the image and removes all spots that size and smaller.

During the raster-edit stage, you can also clean up lines or portions of the drawing that run together. Although the system automatically recognizes Leroy, typewriter, and neatly printed text, you may have to use the editor to identify portions of carelessly hand-lettered text. In addition, you can view any part of the image or send it to the plotter at any time before, during, or after the raster-edit stage.

From the raster stage the system may convert any or all parts of a drawing to vectors. In vector mode, the system functions much as a CAD system does. You can manipulate the image with such editing facilities as move, copy, delete, and create. When the drawing is complete, the system lets you convert it into Initial Graphics Exchange Specification (IGES) format.

The manufacturer claims that in 45 minutes to one hour you can transform a typical D-size, hand-drawn engineering diagram into IGES format. The system also allows conversion from vector to raster form. Regardless of the operation performed, the CRT displays the progress. The CRT also monitors the image as the initial scan occurs.

Model 3000 uses charge-coupled devices for image sensing. The scanner provides 200-dot/in. resolution, and you can set a variable threshold to compensate for the darkness of the document being scanned. The base system sells for \$180,000 and includes a 30M-byte Winchester-disk drive, 1/2-in. tape drive, and a 2.7M-byte floppy-disk drive.

—Maury Wright

Optiguaphics Corp, 4380 Jutland Dr, San Diego, CA 92117. Phone (619) 270-4942.

Circle No 727

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LEADTIME INDEX

Percent of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last months average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	0	29	29	35	0	7	10.7	10.4
Pot-Core	0	29	43	14	7	7	10.3	13.7
Laminate (power)	0	29	42	29	0	0	8.6	9.4
CONNECTORS								
Military panel	0	43	14	29	7	7	10.6	13.6
Flat/Cable	0	52	32	16	0	0	6.2	7.4
Multi-pin circular	0	19	13	43	25	0	15.0	13.0
PC	5	28	45	12	5	5	8.9	6.8
RF/Coaxial	7	39	39	15	0	0	6.3	7.8
Socket	6	55	33	6	0	0	4.7	5.8
Terminal blocks	16	28	39	17	0	0	6.4	8.9
Edge card	0	33	53	14	0	0	7.1	6.4
Subminiature	0	14	57	29	0	0	9.5	7.3
Rack & panel	0	22	45	33	0	0	9.3	11.1
Power	0	42	29	29	0	0	7.8	10.3
PRINTED CIRCUIT BOARDS								
Single sided	0	45	45	10	0	0	6.1	6.4
Double sided	0	29	61	10	0	0	7.1	7.1
Multi-layer	0	32	47	21	0	0	7.8	8.8
Prototype	5	90	5	0	0	0	2.2	3.5
RESISTORS								
Carbon film	39	36	18	7	0	0	3.3	4.7
Carbon composition	25	40	20	5	10	0	5.8	6.7
Metal film	18	41	18	23	0	0	5.9	6.6
Metal oxide	15	31	46	8	0	0	5.6	6.7
Wirewound	10	20	60	10	0	0	6.8	8.7
Potentiometers	6	42	29	23	0	0	6.8	8.2
Networks	9	32	41	18	0	0	6.8	8.6
FUSES								
	19	42	27	12	0	0	4.9	4.4
SWITCHES								
Pushbutton	13	26	48	13	0	0	6.4	8.1
Rotary	13	19	43	25	0	0	7.8	10.0
Rocker	6	38	44	12	0	0	6.2	4.8
Thumbwheel	0	20	60	10	10	0	9.4	10.6
Snap action	17	50	25	8	0	0	4.3	7.9
Momentary	0	50	25	25	0	0	7.0	7.3
Dual-in-line	17	33	33	17	0	0	6.0	5.7
WIRE AND CABLE								
Coaxial	21	58	21	0	0	0	2.8	4.1
Flat ribbon	21	50	29	0	0	0	3.3	3.6
Multiconductor	18	41	41	0	0	0	4.1	6.1
Hookup	45	35	20	0	0	0	2.3	3.1
Wirewrap	55	27	18	0	0	0	2.0	3.9
Power cords	16	56	20	8	0	0	4.0	5.8
Other	0	75	25	0	0	0	3.5	6.0
POWER SUPPLIES								
Switcher	0	21	29	36	7	7	12.5	14.8
Linear	0	42	25	25	8	0	8.9	12.0
CIRCUIT BREAKERS								
	0	16	58	26	0	0	9.1	11.0
HEAT SINKS								
	5	42	32	21	0	0	6.8	10.8

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last months average (weeks)	Average (weeks)
RELAYS								
General purpose	16	20	52	12	0	0	6.5	8.2
PC board	0	24	41	35	0	0	9.4	10.4
Dry reed	0	50	50	0	0	0	5.0	10.6
Mercury	0	25	75	0	0	0	6.5	9.2
Solid state	0	33	25	33	9	0	10.3	10.3
DISCRETE SEMICONDUCTORS								
Diode	15	42	30	12	0	0	5.2	6.9
Zener	15	40	37	7	0	0	4.9	7.4
Thyristor	0	54	31	15	0	0	6.0	9.1
Small signal transistor	6	39	39	16	0	0	6.5	8.6
FET, MOS	0	33	27	27	13	0	10.5	10.4
FET, bipolar	0	29	43	14	14	0	9.9	11.2
INTEGRATED CIRCUITS, DIGITAL								
CMOS	4	30	22	37	7	0	10.1	10.1
TTL	14	27	23	36	0	0	8.1	8.9
LS	15	30	25	25	5	0	7.9	8.7
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	9	36	46	9	0	12.8	11.0
OP amplifier	0	23	46	27	4	0	9.5	10.5
Voltage regulator	0	30	39	26	5	0	9.2	10.7
MEMORY CIRCUITS								
RAM 16K	17	33	33	17	0	0	6.0	9.9
RAM 64K	6	38	31	19	6	0	7.8	8.4
RAM 256K	11	0	67	11	0	11	10.5	9.1
ROM/PROM	0	30	40	10	20	0	10.6	9.5
EPROM	7	33	40	13	7	0	7.8	7.9
EEPROM	0	29	29	28	14	0	11.0	8.3
DISPLAYS								
Panel meters	0	23	54	23	0	0	8.5	9.5
Fluorescent	25	0	0	75	0	0	12.0	14.6
Incandescent	50	0	10	50	0	0	8.0	7.2
LED	5	21	32	42	0	0	9.7	9.2
Liquid crystal	0	0	29	71	0	0	13.7	7.8
MICROPROCESSOR ICs								
8-bit	0	20	33	40	7	0	11.3	9.9
16-bit	11	11	34	33	11	0	11.1	10.9
FUNCTION PACKAGES								
Amplifier	0	17	66	17	0	0	8.4	11.5
Converter, analog to digital	0	33	50	17	0	0	7.4	9.5
Converter, digital to analog	0	43	43	14	0	0	6.5	13.1
LINE FILTERS								
	0	9	73	18	0	0	8.9	9.5
CAPACITORS								
Ceramic	24	28	40	8	0	0	5.0	5.3
Ceramic monolithic	10	25	35	30	0	0	8.1	7.4
Ceramic disc	16	36	32	16	0	0	5.8	8.3
Film	0	25	50	25	0	0	8.5	6.8
Electrolytic	7	29	39	25	0	0	7.7	8.3
Tantalum	11	11	48	26	4	0	9.3	10.3
INDUCTORS								
	5	16	53	26	0	0	8.7	7.9

Source: Purchasing magazine's electronic business survey

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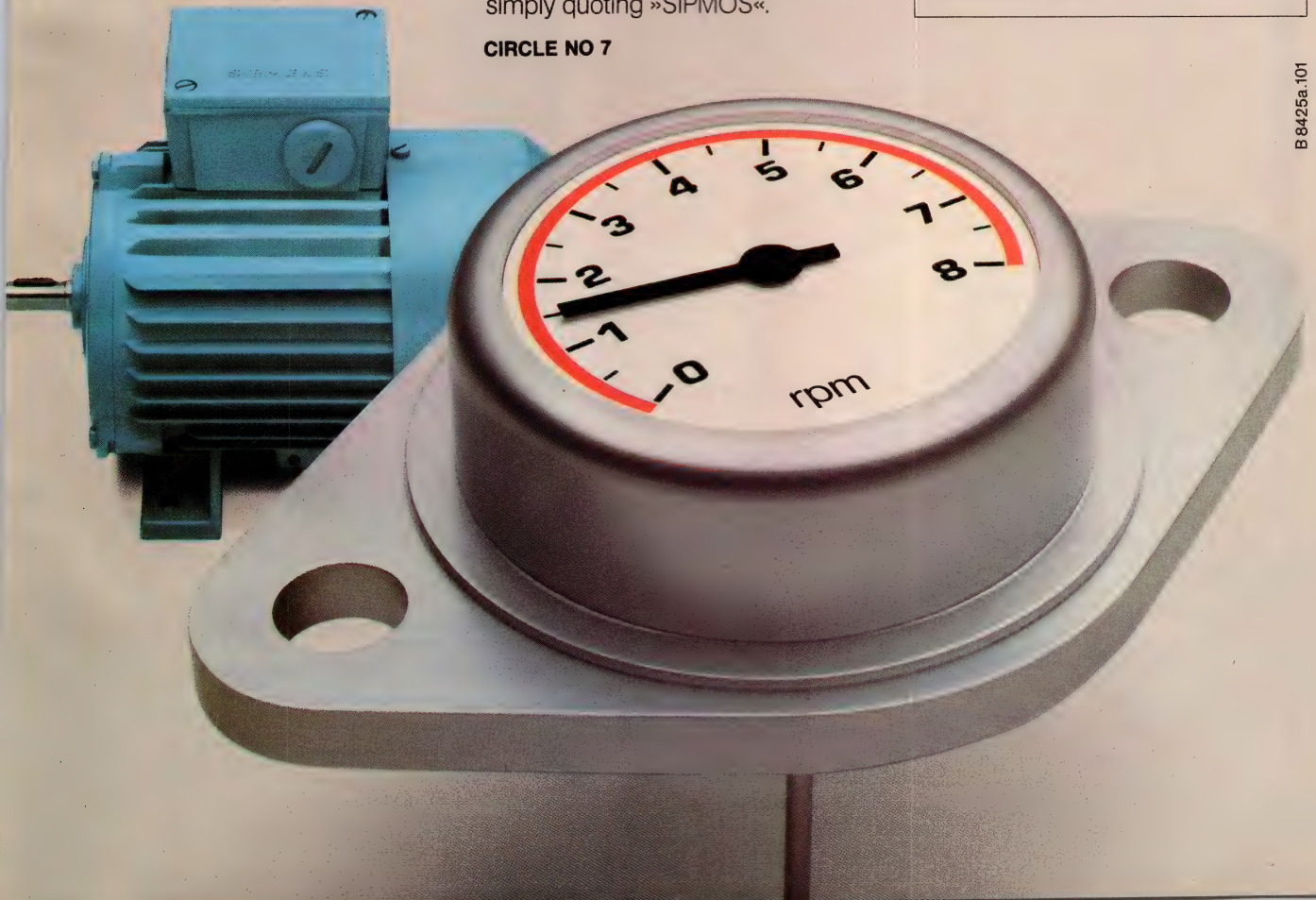
CIRCLE NO 7

*SIPMOS – Siemens Power MOS

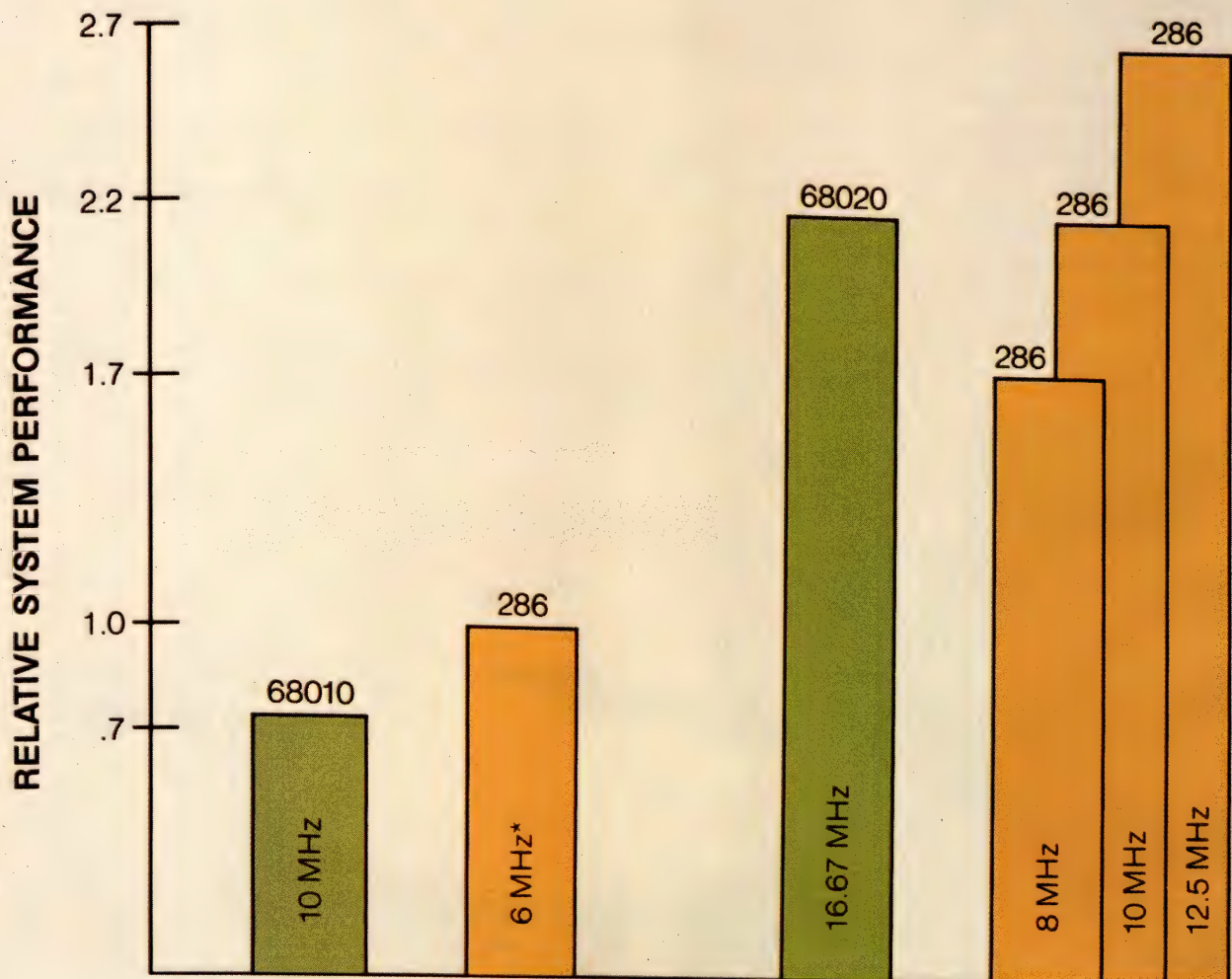
is the power-semiconductor technology that sets standards.

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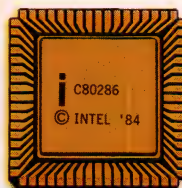
	iAPX 286	68020
PIPELINING		
Register memory moves	Avg. Clock/Inst. 5	Avg. Clock/Inst. 7.9
Arithmetic and logic instructions	4.75	7.5
Conditional jumps	7	6.5
ON CHIP MMU	YES	NO
TASK SWITCH	13.5 μ s	Up to 10X slower (Software dependent)
EFFICIENT BUS		
Memory to memory move	6MB/SEC	5.2 MB/SEC
COPROCESSOR SUPPORT (in volume production)	Numerics-80287 I/O-82258 LAN-82586 Graphics-82730	DMA-68450

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Development systems for 32-bit μ Ps

With the introduction of 32-bit μ Ps, a microprocessor development system will no longer be limited to a single-user host coupled to an in-circuit emulator. Now such tools can range from software development systems made from board-level products to high-speed bit-slice hardware-development equipment.

Charles H Small, Associate Editor

Developing a product that incorporates a 32-bit μ P is a completely new ballgame, whether you're moving down from superminicomputers or moving up from 8- and 16-bit systems. What distinguishes a 32-bit- μ P project from all other μ P development projects is the target system's increased complexity (of both hardware and software), cost, and power.

These aspects affect the two groups of developers differently. For the developer whose previous experience is with 8- or 16-bit μ Ps, the 32-bit projects will entail vastly more complicated hardware and software. These developers will now confront challenges previously reserved for mainframe-computer developers. In

Developing products that incorporate 32-bit μ Ps should prove to be an out-of-this-world experience that differs significantly from projects based on either superminis or 16-bit μ Ps. However, a variety of tools, ranging from emulators to board-level target hardware, can help you bring the task down to earth. (Photo courtesy Motorola)

many cases they will for the first time have to deal with cache memory, memory management, multiuser/multitasking software, and multiprocessor architectures. The wide buses and high clock speeds of 32-bit μ Ps will strain the capabilities of the hardware-based development tools this group is used to.

Supermini users move on

Those who have developed large software systems on superminis and want to take advantage of lower-cost 32-bit- μ P systems will find themselves working in unfamiliar territory as well. Particularly, they will be able to develop software on the target system itself, because that target system is so powerful. Typically, these developers have to share the supermini resource fairly with a multitude of users in other departments.



Combining a ROM emulator, a logic-state analyzer, a pattern generator, and a hard-disk-based computer, the Step Engineering Step 27 can work with the fastest 32-bit μ Ps.



The NCR32 32-bit μ P is a microprogrammed processor and, hence, mandates a development tool like the Hilevel DS370 ROM emulator and logic analyzer rather than an in-circuit emulator. However, because of their high speed and flexibility, ROM emulators also suit nonmicroprogrammed μ Ps like the 68020 and 32032.

No one user may monopolize the supermini's facilities or damage other users' programs. Consequently, the supervisory software on a supermini must strictly protect and isolate the hardware from the users. Indeed, this practical necessity that programmers keep their hands off the native machine has been raised to an article of faith among computer scientists. They maintain that high-level-language programmers should never have to deal with the real nature or peculiarities of the computer they're working with.

Inexpensive, plentiful 32-bit- μ P systems will revolutionize the way this group interacts with target systems. Unlike previous inexpensive computers based on 8- or 16-bit μ Ps, 32-bit- μ P systems have the execution speed and addressing range to handle the most sophisticated software tools, and they still have plenty of room left over for the application code. Because 32-bit- μ P systems won't be expensive, each programmer—or small team of programmers—can have exclusive use of one machine. Consequently, programmers can do their development on the target system rather than on a superminicomputer. You can even get a software-development/software-execution vehicle composed of board-

A 32-bit- μ P software-development system assembled from available board-level products, as National Semiconductor's VR32 is, can serve as both a powerful software-development environment and as a software-integration environment that closely mimics that target system.



level products for about the same cost as a single terminal on a DEC VAX.

What's more, because each programmer has his own computer, the requirement for protecting the computer from multiple users goes away. Therefore, the 32-bit- μ P programmer can delve deeply into the workings of his hardware and software by connecting such hardware-based development tools as emulators and logic analyzers, which were previously used only by 8- or 16-bit- μ P programmers. If these hardware-based tools have access to information from the compiler and know how the operating system works, they can provide real-time tracing and trapping, in terms of high-level constructs, of the execution of even the most complex software.

High-level-language programmers developing software on superminicomputers have had no such intimate control over the target system. The best they had to work with was so-called symbolic debuggers that, in essence, transformed their host-system CRT into the controller of a monitor ROM on the target system's CPU board. This monitor ROM gave the programmers rudimentary debugging facilities. With the monitor,

Mainframe-like aspects of 32-bit- μ P projects will strain the ability of conventional instrumentation to keep up.

they could set software breakpoints, perform single-stepping, and examine and change memory and processor registers. The developers couldn't, however, handle interrupts, measure execution times with high resolution, trace and trap on dynamically defined data constructs, or do sequential triggering on complex series of events. Such advanced debugging is possible only with hardware-based debugging tools.

Emulator choices limited

The hardware-based debugging tool most familiar to the developers of 8- and 16- μ Ps is the in-circuit emulator. Currently, your choices for in-circuit emulators for 32-bit systems are as limited as your choices for 32-bit μ Ps. Right now, only Motorola and National have in-circuit emulators for their respective 68020 and 32032 32-bit μ Ps. Prospective 32-bit- μ P vendors like Intel and Zilog have 32-bit emulators in the works but won't announce the development tools until they have chips ready as well. With the exception of Microtek, third-party makers of universal development systems, like Tektronix, Hewlett-Packard, and Philips, think that it's much too early in the 32-bit μ Ps' lives to begin supporting the chips.

The makers of universal development systems supposedly learned from their experience with 16-bit- μ P development systems that the first wave of users of a new class of μ P doesn't need in-circuit emulators. Initially, these companies see the 32-bit μ Ps going into software-intensive workstations. They envision that, though each workstation maker will sell large numbers of workstations, there will not be many such makers. Furthermore, developers of such systems have scant need for real-time tools. Beyond merely getting their target systems to function, these developers will be perfectly satisfied with conventional software-based debugging. By the development-system makers' reckoning, therefore, two or more years will have to pass before there are enough embedded-processor designs (employing 32-bit μ Ps) to make it worthwhile to produce third-party emulators. The R&D commitment would simply be too great at this point.

The specs for Motorola's 68020 emulator pod for its HDS-400 emulator station illustrate just how difficult designing real-time debugging tools for 32-bit μ Ps is. If you plug a 16.67-MHz 68020 into the pod, it can run with no wait states at 8.0 MHz. If you run the processor at its full clock speed, you pick up one wait state with each memory access.

The pod can address any contiguous 16M-byte sector

within the 68020's 4G-byte address space. The HDS-400 provides as much as 256k bytes of emulation memory, which you can map in 4k-byte increments over the target system's memory. According to the company, the pod supports cache-memory operation. Either the target system can control its own cache, or you can use a command from the development system.

The HDS-400 emulator also has a state analyzer that runs in parallel with its emulator. The analyzer has 75 pins committed to the μ P, plus four uncommitted



Because of the multichip architecture of the 32032, National's ICE32 emulator has a cable for the μ P, the memory-management unit, and the clock chip.

inputs with which you can monitor additional nodes in the target system. The state analyzer can keep up with 5-MHz bus transactions in real time; at 20 MHz, the analyzer must insert a 1-cycle wait state.

The development system has two kinds of breakpoints; emulator breakpoints and analyzer breakpoints. The emulator breakpoints include 16 (in four address ranges) that are defined by the state of the μ P, one cross-triggered breakpoint initiated by the analyzer, an autonomous timer breakpoint, and an erroneous-write breakpoint caused by writing to a section of memory designated as ROM. Motorola states that its emulator isn't fooled into breaking on instructions that are pre-fetched but not executed; its emulator breaks prior to an instruction's execution, and only on instructions that would actually have been executed.

Sophisticated triggering a must

Given that most 68020 programs will be complex, sophisticated triggering of the analyzer's capture cir-

cuitry is imperative. As an example of a hardware tool that can provide more power than software debuggers, the HDS-400's optional state analyzer can halt the target system's execution after it sees a preprogrammed sequence of events. This ability to follow a complicated sequence of software events contrasts with the emulator's basic ability to halt on any one of 16 events. The analyzer can monitor a program's execution through a predefined series of as many as seven events. Each event is a state defined across the analyzer's 79 input lines.

Halting the target system is only one capability of the analyzer. It can also selectively capture data as it steps through its trigger sequence. If you set up the analyzer to recognize the entry and exit points of a particular routine, the analyzer can then measure the routine's execution time—with a resolution of one cycle, of course. You can also define 16 address ranges for a software-performance histogram.

A simple feature is the analyzer's ability to record activity *outside* a given range as well as inside it. This capability allows you to find out not only where your program goes but where it doesn't go as well. Analyses of the run-time behavior of large programs reveal two things: the expected overuse of certain modules (candidates for being rewritten in assembly code for greater speed), and the unexpected (ie, modules that never get called at all). The latter are candidates for elimination, or perhaps they're symptoms of poor execution of a top-down design.

National's \$12,900 ICE32 emulates the 32032 32-bit μ P at 6 MHz (later versions will run at the chip's top speed of 10 MHz). The emulator has 128k bytes of emulation memory (not expandable). The emulator looks different from most emulators. Instead of having a single cable with a DIP header for connection to the target system, the ICE32 has three cables; one cable terminates in a dummy leadless chip carrier (LCC), and the other two have more conventional DIP headers.

Hydra-headed emulator

The ICE32 needs three connections to the target system because of the 32000 Series architecture. The 32000 Series has separate CPU and memory-management chips. So that the emulator can meet timing requirements, it contains the CPU, memory-management, and clock-control chips in its pod—hence the three connections to the target system.

With the ICE32, you can set three event breakpoints on either instructions or address fetches. Alternatively,



Sporting an elaborate plug that mates to a 68020 32-bit μ P's pin-grid-array socket, Motorola's HDS-400 emulates the μ P at 8.0 MHz with no wait states.

you can use the three events to break on a range of addresses. The emulator also has a 12-bit counter with which you can count different kinds of processor cycles—memory, instruction, or clock—or breakpoints that delay the halting of the software under test. In addition, you can set a 24-bit counter to time the execution of specific software modules.

The emulator also has a 255-state trace memory. In its program-counter mode, it stores 255 nonsequential program-counter values and keeps a count of cycles occurring between stored events. In memory-bus mode, it captures 255 sequential states of the μ P, including address, data, and status values.

Alone among third-party emulator makers, Microtek Labs is bringing out emulators for the 68020 and Intel's 80286 this year. By press time, the company should have introduced a 16-MHz 68020 emulator. The unit will have 256k bytes of emulation memory and cost less than \$10,000.

Embedded μ Ps strain emulators

Even though these available in-circuit emulators don't run at a 32-bit μ P's top speeds, some beta-site users are already designing-in the 68020 as a high-

Powerful, inexpensive 32-bit- μ P target systems will challenge the fundamental tenets of software engineering.

speed, embedded processor. At first glance, a 32-bit μ P might seem like overkill as an embedded processor. The term "embedded processor" often refers to an 8-bit single-chip μ P that controls, say, a microwave oven or performs a simple task like protocol conversion in a multiprocessor computer. Such is not the case for the 68020's embedded applications. The embedded-processor designs it's being considered for are applications that would otherwise require a bit-slice processor.

The 68020 is fast, handles wide words, does bit manipulation and barrel shifting of those long words, and can perform a 64×32 -bit unsigned divide in 5 μ sec. Although it's not as fast as a bit-slice processor and can't be microcoded for optimizing specific tasks, the 68020 takes up far less room and consumes far less power. Furthermore, the hardware design and debugging time is shortened for an integrated 68020 vs the multitude of chips that compose a bit-slice design.

Using a 68020 or another 32-bit μ P in designs that previously could have been done only with bit-slice processors mandates the use of some sort of real-time debugging tool. ROM emulation is the standard technique employed in bit-slice-processor development, but it's presently not very common for μ P development. However, many of the most difficult aspects of bit-slice development are similar to those of 32-bit μ P development. Specifically, such tasks include the measurement and characterization of the performance of high-speed processors, wide data and address buses, and custom configurations of target systems. Therefore, those who have used only in-circuit emulators for their 8- and 16-bit designs should take a fresh look at bit-slice development tools for their 32-bit μ P development projects.

It's a fact of physics that emulating a processor with a cycle time of less than 100 nsec is difficult. Bit-slice processors have always run at such speeds, and most semiconductor makers state that they will eventually have 32-bit μ Ps that will be almost as fast. If you try to remove such a processor from its socket and make it run in a pod at the end of a 12- to 18-in. cable, signal delays down the cable may violate the target system's timing requirements. Furthermore, a major purpose of putting the emulation μ P in the pod is to let the emulator switch the emulation μ P's I/O and memory lines back and forth from the target system's memory to the emulator's emulation memory. Recognizing when to switch the processor's lines and effecting the change in time is very difficult at the high speeds of 32-bit μ Ps.

Like 32-bit μ Ps, bit-slice processors have wide buses—quite a bit wider than 32 bits, in fact. It's very common for a bit-slice processor's microcode word (the bit-slice equivalent of an op code) to be 128 bits wide. Some designs exceed 256 or even 512 bits. In addition, a bit-slice design doesn't have a predetermined configuration for the processor.

ROM is key to target system

Because of these characteristics, designers of bit-slice development systems have chosen to gain control of the target system, not by emulating the processor, but by emulating the processor's ROM. This approach has some advantages and some disadvantages when compared with in-circuit emulation. The first advantage is that ROM emulation is easy to do; you can obtain a ROM emulator that has a 10-nsec cycle time (measured at the target-system interface). This speed is far faster than the 8-MHz max clock rate (with no wait states) of Motorola's 68020 in-circuit emulator.

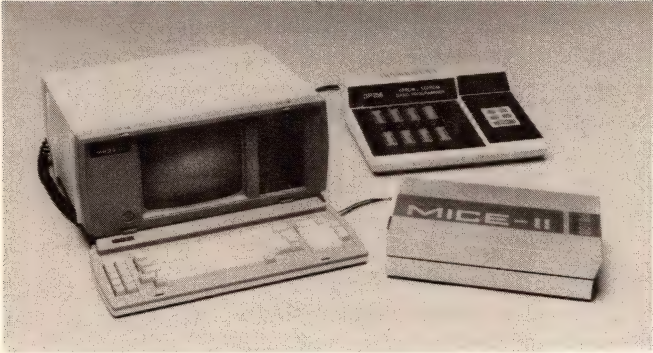
Also, with ROM emulation, the emulator doesn't have to switch the processor's lines back and forth between target-system and emulation memory; the processor is connected to emulation memory all the time. Furthermore, although no two μ Ps are at all alike, all ROMs look pretty much the same. Therefore, you can use a ROM emulator for a wider variety of projects than a processor-specific in-circuit emulator can handle.

Second-hand μ P information

The major disadvantage of ROM emulation is that the emulator does not see activity within the processor. The emulator must infer such activity based on external information. Therefore, to capture the state of the processor, a ROM emulator must recognize an event, halt the processor somehow, and obtain a dump of the processor's state. You can't do this in real time.

Note, however, that 32-bit μ Ps have built-in debugging modes that allow you, for example, to single-step them and easily dump their registers. Earlier 8- and 16-bit μ Ps had no such special control modes. Therefore, 8- and 16-bit in-circuit emulators employed special-purpose hardware in the pod—or even special bond-out versions of the μ Ps—to effect such debugging functions. With a ROM emulator, you can easily access the 32-bit μ P's built-in debugging facilities from an idle loop inserted into the target system's program in emulation memory.

ROM emulators employ two basic schemes to gain



Currently, the only noncaptive in-circuit emulator for 32-bit μ Ps comes from Microtek Labs. The company's units emulate the 68020.

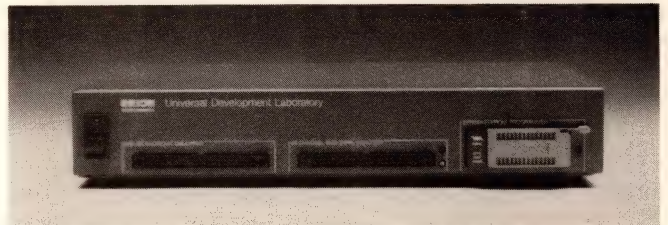
control of the processor. One is to replace an instruction in the program under test with a Jump instruction to a diagnostic routine (idle loop) or with a Halt instruction. Alternatively, if the emulator has an optional logic analyzer installed, the analyzer's trace and trap circuitry can toggle an emulator-output line that gates the target system's clock on or off.

Now that Advanced Micro Devices (the originators of the bit-slice processor) has bowed out of the bit-slice development-system business, only two vendors remain: Hilevel Technology and Step Engineering. Both companies are convinced that their equipment suits 32-bit development.

ROM emulator choices limited, too

In fact, Hilevel Technology has been supplying development systems for NCR's 32-bit μ P, the NCR32. In the case of the NCR32, designers have little choice except to use a bit-slice development tool; the NCR32 is microcoded. In practice, NCR32 developers haven't restricted the use of Hilevel Technology's Emulyzer (emulator plus logic analyzer) to just the chip's microcode ROM; the developers emulate their target system's ROM with the instrument as well. They do so because, although you should theoretically get the microcode (which executes op codes) running correctly before you begin assembling or compiling programs into op codes, in practice it's often not until you begin running higher-level code that you find errors in the microcode. When emulators take the place of both the microcode ROM and the target system's ROM, fixing errors and trying out the repairs becomes much easier than when the microcode is burned into ROMs.

Hilevel acknowledges that the NCR32's external microcode ROM is an exception to the current run of 32-bit μ Ps. Neither the 68020, the 32032, the 80286, nor the Z80000 has external microcode ROMs. Neverthe-



Because the instruments are designed for emulating ROMs in 8- and 16-bit systems, you would need a pair of Orion's \$2395 UDLs to work with 32-bit μ Ps.

less, the company thinks that the latter phases of NCR32 development demonstrates that ROM emulation can compete with in-circuit emulation in both performance and price. For example, to handle a 68020, you'd need at least a 32-bit $\times$ 64k-word ROM emulator. Such a system would cost \$14,000. An 80-bit $\times$ 4k-word state logic analyzer would add \$12,500. Adding a \$2200 timing analyzer (with 15-nsec resolution) would provide not only timing analysis but also a time stamp with which the instrument can calculate software-performance histograms. (Hilevel also thinks that ROM emulation especially suits developing embedded-processor designs.)

Hilevel Technology also supplies emulator-control software that runs on either the IBM PC or a DEC VAX. The control software does expected chores like downloading programs to the emulator's emulation memory and sending commands to the emulator and logic analyzer, and it accesses the symbol tables of common compilers. That way, you can program the emulator to trace and trap on symbolic names rather than raw hex addresses, data, and condition codes.

Emulator includes computer

At \$35,000, Step Engineering's top-of-the-line Step 27 costs more than a Hilevel Technology Emulyzer with roughly equivalent emulation and logic-analysis capabilities. The Step 27 costs more because it's a 68000-based Multibus computer as well as a ROM emulator. The unit includes 512k bytes of computer memory, a

ROM emulators gain control of the system under test by simulating the system's ROM rather than the microprocessor.

10M-byte hard disk, a floppy disk, four serial ports, a Multibus expansion port, and a Centronics printer port. You must supply a CRT terminal. The system runs under the CPM-86K operating system and comes with a 68000 C compiler and a 68000 assembler. (The company also has less expensive models featuring either less powerful computers or just the emulator and no computer at all.)

The Step 27 can emulate ROMs (at their sockets) at 40 MHz, recognize events and control the target system's clock at 20 MHz, and do pattern generation at 35 MHz. It's highly modular and accepts a wide range of ROM-emulation and logic-analysis boards. For a unit that suits 68020 development, a \$35,000 Step 27's instrumentation comprises a 32-bit $\times$ 16k-word ROM emulator and a 54-bit $\times$ 16k-word state analyzer. The state analyzer features 16 levels of sequential triggering, and each level has five 54-bit-wide word recognizers active simultaneously. The price also includes cabling. At extra cost, you can obtain pattern-generator boards. Step offers either a simple sequential pattern generator or one having rudimentary algorithmic pattern generation.

At press time, neither Hilevel nor Step had processor-specific software for setting up the analyzers or decompiling captured data. Such software is easily within the capabilities of both machines' bit-slice software and will probably be on the market soon.

Not all ROM emulators on the market were designed for bit-slice applications. For example, at \$2395, Orion Instruments' 8k-byte UDL ROM emulator is by far the least expensive ROM emulator available. The UDL is not a bit-slice development tool; it was designed for 8- and 16-bit μ P development and, in its present form, can migrate to 32-bit μ Ps with some reservations. The system expands to 32k, 64k, or 128k bytes of 195-nsec response-time memory. The 128k-byte expansion adds \$1395 to the basic price. The emulator's memory appears to the target system as either an 8- or 16-bit-wide ROM. According to the company, the UDL is fast enough to keep up with 20-MHz processors.

The emulator's primary window into the target system is the target system's ROM socket. The emulator also requires approximately 10 additional inputs (depending on the μ P type) to characterize completely the target system's activity. The emulator has a built-in state analyzer. The analyzer features a 4-step sequential trigger, counters, and selective tracing.

The UDL can halt a target-system program's execution in a way that points out the value of combining a

state analyzer with emulated ROM. You can, for example, program the unit to jump to an endless loop when the analyzer recognizes an event. This capability provides a "soft" halt—ie, one that stops the execution of program under test and still leaves the processor running. (This concept is familiar to high-level-software developers who use system monitors for debugging.) In some cases, you may want to keep some aspect of the target system alive even though the program's been halted. In-circuit emulators generally interrupt and halt the target system's processor, which may cause you problems depending on just what the target system is supposed to be doing.

Because the UDL ROM emulator was designed for 8- and 16-bit applications, you would therefore have to parallel two emulators for 32-bit applications. Though each emulator can trace and trap on the 16-bit activity it sees, the pair of emulators has only a single output line. To coordinate two emulators, you would have to make one unit's output line into an input for the other. The success of this scheme depends heavily on the bit patterns in a given 32-bit μ P's op codes.

The company supplies control programs—written in Forth—that run on most common personal computers. Because Forth is an extensible language and because Orion has not hidden the Forth kernel from users, you can extend the control programs with your own programs—if you can program in Forth. The company presently has no software specific to 32-bit μ Ps.

In contrast to the time-critical applications for embedded processors, many applications for 32-bit μ Ps will have few or no time-critical aspects. The critical time for many of these projects will be the time it takes to get a product to market. For these projects, it can make more sense to adopt a development system comprising board-level products than to try—at least initially—to design your own boards from scratch. That way, you can get to work almost immediately and try out your code incrementally as you write it directly on the target system. Developing software on the target system offers a distinct advantage over writing volumes of code on a mainframe and later integrating that code all at once on a target system.

Motorola's initial 32-bit offering comprising board-level products is the Benchmark 20. For \$16,500 you get a 6-slot Versabus backplane (recently upgraded from a 4-slot backplane), a CPU board, and a memory board. The backplane includes a removable front panel and two fans; you provide the power supply. You can also obtain the CPU board and memory board separately.

A state analyzer that has access to the compiler's tables of module and data-construct addresses can trace and trap on high-level software.

The \$6855 VM04 CPU board carries the 68020 32-bit μ P. The board's clock rate is a fixed 16.67 MHz. The board also has a 32-bit $\times$ 4k-word cache memory, memory-management hardware, serial I/O, and a debugging-routine monitor in ROM. Because Motorola's memory-management chip isn't available, the company in the meantime is shipping a small, hybrid board that plugs into the memory-management unit's socket.

The \$4200 VM13 RAM board stores 1M byte (in the form of 64k-byte RAMs) or 4M bytes (in the form of 256k-byte RAMs). To speed memory fetches, the RAM board communicates with the CPU board over a high-speed cable rather than over the Versabus.

The company's latest board-level product is the VME130 CPU board for the VME Bus. Because VME boards aren't as big as Versabus boards, the VME130 doesn't have all the facilities of the VM04. Like the VM04, the VME130 CPU board accepts the hybrid-circuit substitute for the memory-management chip. The CPU board has two 28-pin sockets for 16k bytes of static RAM. Also like the VM04, the VM130 accepts a debugging-routine monitor in ROM.

Motorola doesn't have a packaged VME system, but this shouldn't prove much of a problem, thanks to the large number of vendors offering VME Bus products. Motorola doesn't supply any software beyond the monitor ROM for its CPU boards. If you want to do software development with these boards, you'll have to install an operating system yourself.

National's prepackaged system comprising board-level products is the \$14,500 VR32. The VR32 is a Multibus I computer that includes 500k bytes of main memory, a 40M-byte hard disk, a 1M-byte floppy disk, two serial ports (one for a CRT, the other for controlling an in-circuit emulator), and a Centronics printer port.

The VR32's CPU board is a modified version of the company's \$1895 DB30216 CPU board. This board uses the 16-bit 32016, not the 32-bit 32032. National states that the two chips are code compatible. If you buy the board alone, it comes with a ROM—called the TDS, for Tiny Development System—that has an assembler, linker, and debugging routines for setting breakpoints and single-stepping. Because the TDS code is in the public domain, you can ship it with your product as a testing aid.

Unlike Motorola's system, which has no high-level software installed, the VR32 comes with Genix—National's version of Unix. The Genix system includes an editor, an assembler, a C compiler, and a pair of

The trouble with logic analyzers

All the major logic-analyzer firms have modular logic analyzers that, when stuffed with optional boards, have enough channels and qualifiers to trace and trap on the activity of 32-bit μ Ps. That's the good news.

The bad news is that a fully configured logic analyzer will cost well over \$20,000. Worse yet, only Intech's logic analyzers come with processor-specific hardware and software for 32-bit μ Ps. With all other brands of analyzer, you'll have to set up the analyzer's event recognizers and label display screens yourself so that they match the μ P. Furthermore, you'll have to configure the target-system interface yourself.

What's more, you'll have to write all the post-capture data-analysis software yourself, because—again except for Intech—logic-analyzer makers supply no disassemblers for 32-bit μ Ps.

symbolic debuggers. Each symbolic debugger has its own monitor ROM for your target system. A Pascal compiler costs an extra \$6000.

Because the VR32 runs the same software, employs the same chip set, and controls the same in-circuit emulators as the company's more expensive SYS32 development host (\$31,450), you might wonder whether National is competing with itself. The group that designed National's μ Ps simultaneously designed the SYS32, but the VR32 is based on more recent products from National's board-product division. The SYS32 employs a proprietary, high-speed backplane and can support as many as eight users. The bandwidth of the Multibus limits the VR32 to a single user, even though the software and processor are easily capable of handling several. The company expects that later versions of the 32000-based Multibus CPU boards will have more local memory and will therefore be able to handle more users.

Silicon software stands ready

If you choose to do your development on a system, like Motorola's Benchmark 20, that doesn't come with an operating system, you should consider adding one. Going beyond simple, ROM-based monitors, an operating system in onboard ROM (silicon software, or "siliware") can turn the target system into a development system. Although you could download the operat-

ing system into the packaged target system's RAM each time you switch it on, having the operating system in ROM has two advantages: Programming becomes faster because you don't have to wait for the operating system to load beforehand, and the development system is more robust because the system's operation doesn't depend on reliable operation of the program-communication software and hardware. (Such operating systems must have a slightly different structure than operating systems that reside in RAM and are thus examples of what's called "ROMable" code.)

Luckily, makers of software-development systems for 32-bit μ Ps show none of the reluctance of hardware makers to jump into the market. Predefined operating systems that you can put in a ROM on your target system range from a skeletal set of real-time operating-system calls like Hunter & Ready's VRTX to a full-blown development environment like Forth Inc's 32-bit Polyforth. In fact, you'll soon be able to obtain stripped-down, ROMable versions of elaborate operating systems like Whitesmiths's Idris (a Unix version with real-time extensions).

Perhaps the best reason for adopting a predefined operating system for your target system (to be distinguished from the completely separate issue of choosing a standard operating system for your host development system) is that you can avoid the system programmer's syndrome, which is manifest in the following scenario: A programming team has nine months in which to complete a job and 128k words of program memory to use. Eight months later, the team has written a 124k-word operating system and no application programs whatsoever. A predefined operating system allows your programmers to concentrate on applications.

Skeletal operating system

The least-elaborate ROMable operating system for the 68020 is Hunter & Ready's VRTX. The system costs \$5275 for a 5-copy R&D starter set. The price includes a 1-year warranty, documentation, and one year of maintenance. The price drops to \$70 per copy in lots of 100. The company claims that its system requires almost no customizing to make it fit a target system. Tailoring VRTX to your target system involves writing one page of assembly code.

VRTX is a collection of short routines that your programs can call. The routines perform both real-time and nonreal-time functions. For example, your multitasking program can jump to routines that handle real-time interrupts. The interrupt handlers can use

other calls to post messages for tasks to read, suspend or reactivate tasks, or even change a task's priority. The tasks themselves can use VRTX to send messages to each other. The company also has supplementary systems for nonreal-time tasks like file management.

The kind of multitasking that VRTX enables is very familiar to process-control software engineers and shouldn't be confused with virtual-environment multitasking familiar to high-level-language programmers. That kind of multitasking allows a programmer, for example, to edit a file in foreground mode while compiling or printing out a file in background mode. In this type of environment, each task is a program that operates independently, the programmer cares little about the time that the programs consume, and the tasks do little communicating beyond piping the output of one program to the input of another.

The VRTX system provides only calls for executing applications. There's no development support. To develop programs that use VRTX, the company staunchly supports host-based development. Modifying a host's C compiler so that it invokes VRTX system calls is easy. You can get the necessary hooks for C compilers from the following companies: Hewlett-Packard, Tektronix, Alycyon, Whitesmiths, Greenhills, Intermetrics, Lattice, and Mark Williams.

VRTX isn't presently available for the National 32032. National does have a real-time executive, called Exec. It comes as a 4k-byte module of preassembled code that you can link with your programs. The module provides timer (1-msec resolution), task-scheduling, memory-allocating, and intertask-communication system calls that your programs can use. The company is working on integrating these calls into its C and Pascal compilers.

Industrial Programming's MTOS is similar to VRTX in philosophy—it provides a common skeletal operating system—but it furnishes a richer suite of intertask-communication and -control facilities. The company presently has the 68000 version of MTOS running on the 68020 and plans soon to amend MTOS so that it will work with the special features of the 68020.

Tasks running under MTOS can communicate via bit patterns in global memory (called "event flags" by the company), common memory (called "memory pools"), mailboxes, and semaphores. In addition to allocating memory constructs dynamically, you can also create tasks as the program runs. Under VRTX, you must define all tasks in advance. Furthermore, MTOS can handle as many as 16 μ Ps at once. That way, your

Prepackaged board-level systems save development time if they match the architecture of your eventual target system.

multitasking program can have 16 tasks active at once, with each task dynamically assigned to a processor as needed.

Like Hunter & Ready, Industrial Programming believes in host-based development. Toward this end, one MTOS utility will accept a standard Unix output file (a.out file). This utility makes it easy to download a program from a Unix host to your target system.

MTOS also has links to such software-development tools as debuggers and monitors, as well as high-level languages and file systems. A representative version of MTOS is the \$12,000 package for the 68000-based Omnibyte single-board computer. If you don't need all the source documentation, you can obtain MTOS's object code alone burned into a PROM for the same single-board computer for \$1500 (additional PROM sets are \$350).

Monitor-sized development system

VRTX, MTOS, and National's executive are the underlying skeleton of an operating system. The 32-bit Polyforth package has all the elements of a complete software-development environment. The precompiled Polyforth kernel for 32-bit μ Ps presently occupies 16k words of ROM. In this 16k words, Polyforth has an editor, an assembler, a high-level language, and a multitasking operating system. By comparison, Motorola's 020bug debug monitor comes in a 32k-word EPROM set, and Hunter & Ready's VRTX (with extension) occupies 18k bytes of ROM. What's more, Polyforth's facilities are not separate programs that must be read in and activated one at a time, as with conventional software-development systems. Instead, all these facilities are on line at all times.

You can develop Forth programs on a host or on your target system. All high-level Polyforth I/O calls are vectored to assembly-language routines, so that code written on one computer will run on another. In addition, during the initial stages of a development project, you can use this facility to simulate inputs and outputs to hardware under development by redirecting the vectors to software-simulation routines. When a prototype of the hardware is available, you need rewrite only the assembly-language handlers. Forth Inc provides an ancillary product called the Target Compiler that takes care of the differences between a host computer and the target system, such as I/O port addresses and RAM/ROM boundaries.

The chief strength of Forth is the speed with which you can write and try out code. Because Forth is

interpreted, the compilation of your program is not a complicated translation process. The Forth compiler only needs to find the addresses of the Forth modules (or Forth "words") that you're invoking and put them in an executable list. However, unlike other interpreted languages, such as Basic, you're not limited to the functions that come with the language. You can easily add both your own words and even words that define other words (like DIM in Basic and Fortran). And if you are doing development on your target system, you can take advantage of the fact that Forth makes no attempt to protect the target system from your mistakes; all the resources of the target system are directly available. What's more, Forth wastes no time performing frills (unless you add them) like range checking, type checking, or memory-bounds checking.

Not all projects are successful

The chief disadvantage of programming in Forth is that it necessitates a different style of programming than that suitable to other high-level languages. Good Forth programming style demands top-down, hierarchical partitioning of a problem into Forth words that have only one function. Because the Forth interpreter has no intelligence and cannot deduce anything about the meaning of a word from its context, your extensions—like the kernel that comes with Forth—must be unequivocal. When Forth gurus mandate that each Forth word do only one thing, they mean what they say in the strictest terms.

This programming style is completely foreign to most high-level-language programmers. For example, the typical Unix programmer defines "one thing" much more loosely. "The essence of a Unix shell command is this: It does one thing, and multiple options let the user modify the characteristics of the basic operation to customize the command" (Ref 1).

High-level-language programmers aren't the only ones who have trouble with Forth. Assembly-language programmers who fail with Forth often do so because they try to use the Forth kernel as an assembly language. These programmers attempt to write a straight-line sequence of code and don't employ Forth's inherent structured-programming nature.

Minimal system costs less

The strict minimalism of Forth may or may not pay off in terms of quickly written programs that run fast and don't take up much memory—despite what Forth proponents claim. There's no doubt that the minimalism



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ROM-based development-system software allows even a special-purpose, embedded-processor target system to serve as a development system.

pays off in terms of low initial costs. Forth Inc, for example, sells a full multitasking system with editor, assembler, and target compiler for \$3200—a price that's an order of magnitude less than that of real-time Unix systems. And unlike that of any other software system, Forth Inc's price includes a copy of all the source code. Having the source code proves useful when you're debugging programs with instrumentation, because you know not only the addresses of your program constructs but also the addresses of routines in the operating system.

Unix needs work

Unix is all the rage as a software-development environment. As an *execution* environment, it's sadly lacking in the facilities needed to survive in the real world. Unix lacks—among other things—security, sequential files, and real-time processing. Unix operating systems with real-time extensions attempt to remedy these shortcomings so that you can employ Unix as both a development and execution vehicle.

For example, both Whitesmiths's Idris (based on Unix version 6) and Alcyon's Regulus (based on Unix System V in the latest release) have a prioritized, real-time scheduler appended to the native Unix scheduler. The companies are currently implementing the necessary modifications to tailor the systems to the 68020 32-bit μ P. These versions should be available by the second or third quarter of this year.

Real time for real world

The native Unix scheduler suits only the narrow, idealized world of program development. Each Unix user has the same priority and is assigned a fixed slice of the processor's time on a round-robin basis. A task is interrupted, whether it's finished or not, when its time slice elapses. The scheduler is deemed successful if it responds to an interrupt within a human's threshold of perception ($\frac{1}{30}$ sec). The real-time extensions to Unix allow a high-priority task to respond directly to an interrupt instead of letting a largely autonomous I/O system herd the tasks' messages in and out of a pool of buffers. The real-time task can monopolize the processor until it finishes its job. As conditions change, the real-time scheduler can reorder tasks' priorities.

Furthermore, because regular Unix users are individuals working on their own files, there's little need for intertask (interuser) communication beyond electronic mail or piping the output of one task into the input of another task. In contrast, the real-time extensions have

mechanisms for fast, intimate, intertask communication and control. As a consequence, these real-time operating systems suit engineering applications far better than do plain Unix operating systems.

Alcyon charges \$42,000 for a license for 600 copies of Regulus. The fee includes one year's maintenance. If you want the source code so that you can trace and trap on operating-system activity or customize the operating system, you'll have to pay an additional \$22,000 for it. In a surprising turnaround, rather like Volkswagen of Brazil exporting cars to Germany, the company reports that AT&T has licensed Regulus for some smaller computers.

Scheduler consumes overhead

As for performance, the Regulus real-time scheduler does, of course, add overhead. Performance figures aren't available for the 68020, but a system call takes a minimum of 60 μ sec on a 10-MHz 68000.

Whitesmiths's pricing for its Idris operating system isn't as clear cut as Alcyon's. A representative price is the \$15,000 single-copy fee for Idris on the Omnibyte 68000-based workstation. Whitesmiths also details a performance benchmark obtained from the Omnibyte system. The company set up a pair of independent tasks that communicated on a 38.4k-baud loop-back serial line. Each character transmission involved a sequence of events: The transmitting task requested a transmit system call that invoked a transmit-interrupt handler, and the receiving task requested a receive system call that invoked a receive-interrupt handler. Idris transferred 240 cps and simultaneously processed 50 timer-task interrupts per second.

Unix versions are large

In addition to dealing with the slow response time of most nonreal-time versions of Unix, you'll have to contend with their alarming size. For example, the IBM PC implementation of a small-system Unix variant (Venix) consumes 192k bytes of RAM for the kernel, and on-line utilities consume an additional 3.5M bytes of disk storage for library routines. Versions of Unix for superminis are even larger and can consume 500k bytes of RAM and 16M bytes of disk space.

The fact that most Unix versions have a large code size and low performance is easily understood when you remember that they were written in a high-level language: C. However Uniflex—a *Unix-like* operating system—from Technical Systems Consultants is written in 68000 Series assembly language. Consequently,

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Adopting a predefined operating system for your target system will allow your programming team to concentrate on applications.

Uniflex takes up 68k bytes of RAM and 1.7M bytes of disk space. The company asserts that Uniflex runs much faster than other Unix or Unix-like systems.

Uniflex costs \$550, including a C compiler and C library. Basic, Fortran, Pascal, assemblers, and various other utilities are extra. The company plans to field a ROMable version of Uniflex within a year, but at this time it has no plans to append real-time extensions to Uniflex.

You can obtain Uniflex installed on a 68020-based multiuser system from Gimix. A base version of the GMX 68020 costs \$13,680.20 and comes with 512k bytes of RAM (expandable to 1M byte), three intelligent serial ports, a 1M-byte floppy disk, and a 19M-byte hard disk.

Consider common operating system

An examination of the costs for these software-development systems reveals two reasons why having a common operating system on the host development computer and the target system makes sense: First,

you could easily spend far more than these operating systems cost in writing and maintaining your own operating system (to find out just how much more, translate Regulus's \$42,000 into programmer man-months at your company's rate). Second, with the same operating system on the host and target systems, programmers should have no problems when moving a program from the host to the target.

Whether you buy a standard operating system for your target system or write your own, software-development systems for your host will be plentiful from both third-party vendors and the μ P vendors. For example, Boston Systems Office plans to introduce cross assemblers, cross compilers, and symbolic-debugging programs for the 68020 during the third and fourth quarters of this year. Systems & Software Inc will extend its Softprobe/87 (a software simulation of Intel processors) to the 80286 by the fourth quarter of this year. Softprobe/87 runs on DEC VAXs under either VMS or Unix (System III, System V, or Berkeley 4.2).

Compensating for a lack of third-party support,

Manufacturers of 32-bit- μ P development tools

For more information on 32-bit- μ P development tools, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Alcyon Corp

8716 Production Ave
San Diego, CA 92121
(619) 578-0860
Circle No 699

Boston Systems Office

469 Moody St
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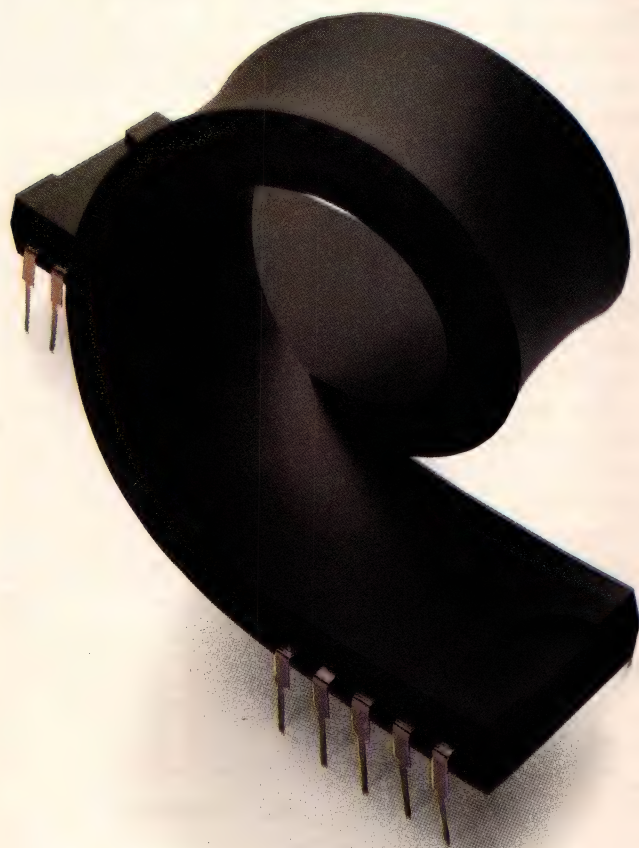
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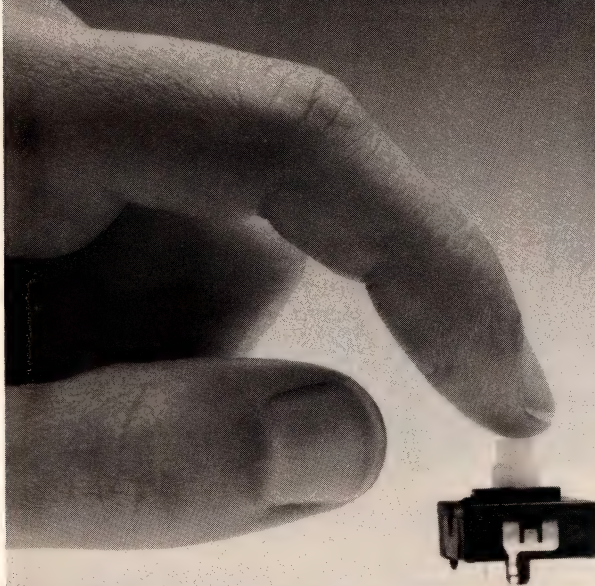
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National is offering a wide range of software products. Genix, the firm's version of Unix, costs \$30,000 for a source license for custom installations and \$10,000 for a version that will run on DEC VAXs under either VMS or Berkeley 4.2 operating systems. Genix includes a C compiler, cross assembler, linker, library routines, programmer utilities, emulator-control routines, and two kinds of symbolic debuggers. You can obtain a Pascal compiler for an additional \$6000.

For host computers other than the VAX, National depends on other vendors. Solutionware has National's development software in versions that will run on Z80-based CP/M computers. Similarly, JMI Software Consultants handles an IBM PC version, and Softrade International works with the DEC PDP-11 running the RSX-11 operating system.

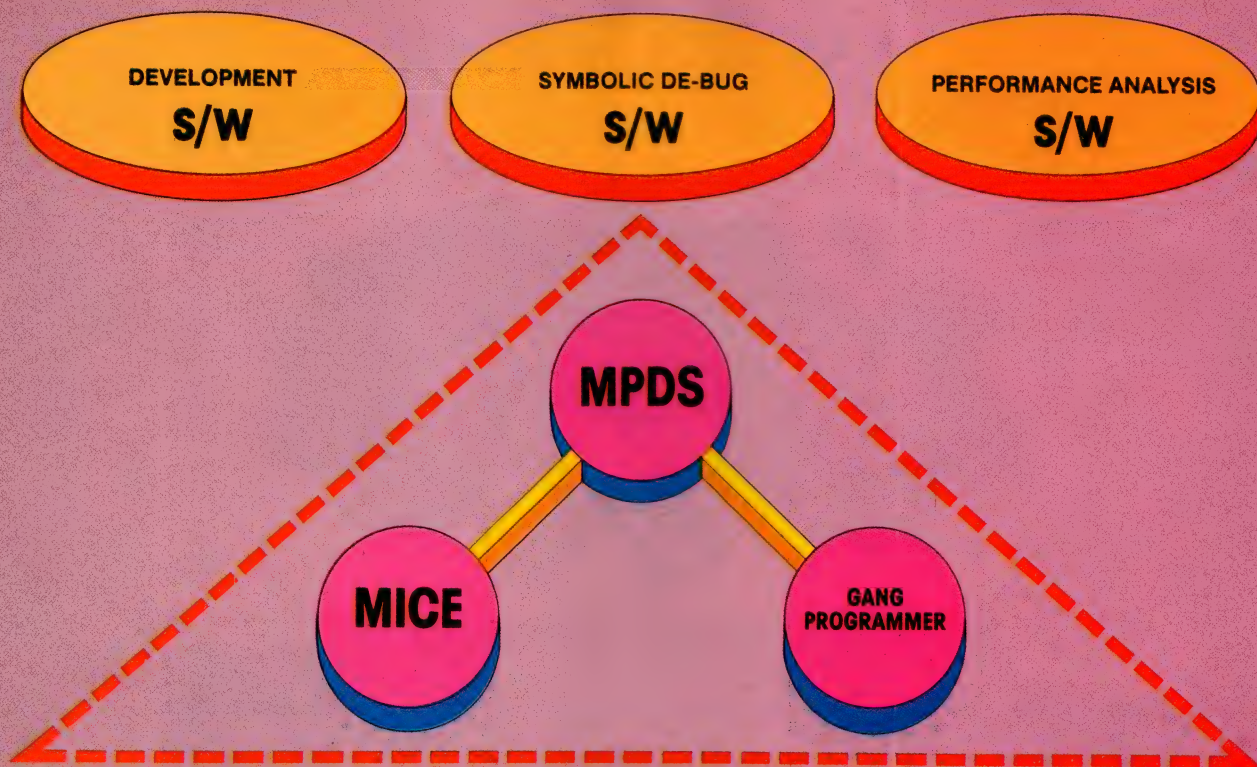
Motorola currently has only an assembler for the 68020. The assembler runs under the company's proprietary Versados operating system or under its System V/68 (a derivative of Unix). The macroassembler supports not only the 68020 CPU chip but also the associated floating-point processor. The assembler will also generate code for the 68000 and 68010. Executable versions cost \$600, and the source code costs \$5000.

Motorola provides links to three different computers, upon which you can do software development and control the company's emulator. The three computers are the Motorola VME/10 (a single-user system), the Motorola Exormacs (a 4-user system), and the DEC VAX. For each computer, the company has assemblers, compilers, and emulation-control programs. **EDN**

Reference

1. Brouwer, Peter, "Developing a Unix Command," *Attage*, March/April, 1985, pg 53.

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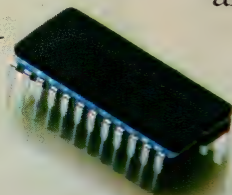
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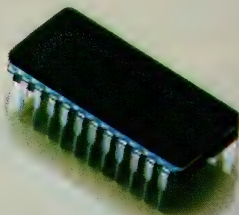
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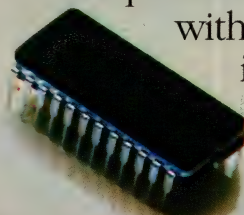
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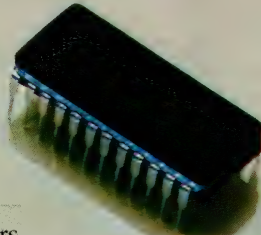
2 Years



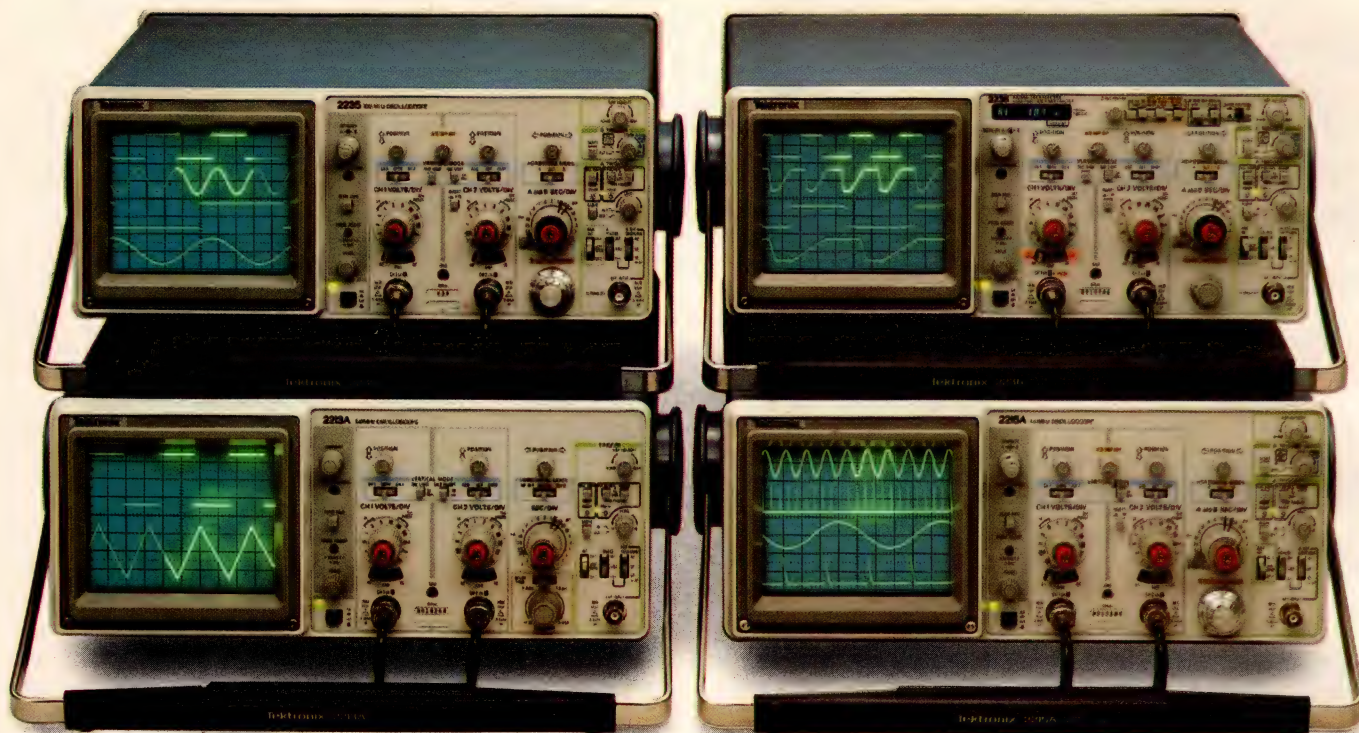
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6 Years



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Bandwidth	60 MHz	60 MHz	100 MHz	100 MHz
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Alternate Sweep	—	Yes	Yes	Yes
Vert/Trig — B/W Limit	Yes — 10 MHz	Yes — 10 MHz	Yes — 20 MHz	Yes — 20 MHz
Single Sweep	Yes	Yes	Yes	Yes
Accuracy: Vert/Horz	3%	3%	2%	2%
Delay Jitter	1:10,000	1:20,000	1:20,000	1:10,000
Triggering Sensitivity	0.3 div at 5 MHz	0.3 div at 5 MHz	0.3 div at 10 MHz	0.35 div at 10 MHz
Input R-C	1M Ω —20pf	1M Ω —20pf	1M Ω —20pf	1M Ω —22pf
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Integrated Counter/Timer/Multimeter	No	No	No	Yes

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Follow design rules for optimum use of fast comparator IC

To fully exploit a high-speed comparator IC's capabilities, you must understand both the IC's innate attributes and the influences of the circuit environment surrounding the device. This article, first in a 3-part series, explores these attributes and influences, and provides guidelines for optimizing high-speed circuit performance.

Jim Williams, *Linear Technology Corp*

A recent high-speed comparator, the LT1016, offers complementary, TTL-compatible outputs and 10-nsec response time. The outputs directly drive all TTL families, including high-speed AS and Fairchild Advanced Schottky TTL (Fast) parts. The TTL outputs make the device easy to use in linear-circuit applications, where ECL output levels are often inconvenient. This article, first of a 3-part series, covers application and measurement techniques and discusses a number of problems associated with the high-speed circuitry the LT1016 would normally inhabit. The other two articles

will provide a variety of circuit applications that exploit the device's capabilities.

The LT1016 is relatively easy to use; it's less prone to oscillation and other vagaries than some other comparators (see **box**, "A fast TTL comparator"). Unfortunately, the laws of physics dictate that you properly prepare the circuit *environment* in which the device works. The performance limits of high-speed circuitry often stem from layout considerations or from such parasitic effects as stray capacitance and ground impedance. Some of these considerations also exist in digital systems, in which you're perfectly comfortable describing bit patterns and memory-access times, for example, in terms of nanoseconds.

The LT1016 is, of course, useful in the mentioned fast digital systems; **Fig 1** gives an idea of just how fast the device is. The simple test circuit allows you to see that the comparator's response (trace B) to the pulse generator's output (trace A) is faster than that of a TTL inverter (trace C). In fact, the inverter's output never attains a TTL zero level. Linear circuits that operate with this order of speed make many designers justifiably wary. Nanosecond-domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation, and outright failure to function.

Among other common problems of such high-speed

To use a high-speed comparator effectively, you must understand not only the IC itself, but also the influences and vagaries of the circuit environment surrounding the device.

linear circuits are differing measurement results when you use various pieces of test equipment, the inability to make measurement connections to the circuit without inducing spurious responses, and dissimilar operation between two supposedly identical circuits. When a circuit's design and the components used in it are sound, you can usually trace all the cited problems to an improper circuit environment. To provide a proper

environment, you must study the causes of the mentioned difficulties.

The most common high-speed-circuit problem is improper power-supply bypassing. Bypassing is necessary to maintain low supply impedance. Inductance and dc resistance in supply wires and pc-board traces can easily attain unacceptable levels. These parasitics allow the supply line to fluctuate in response to changes in the

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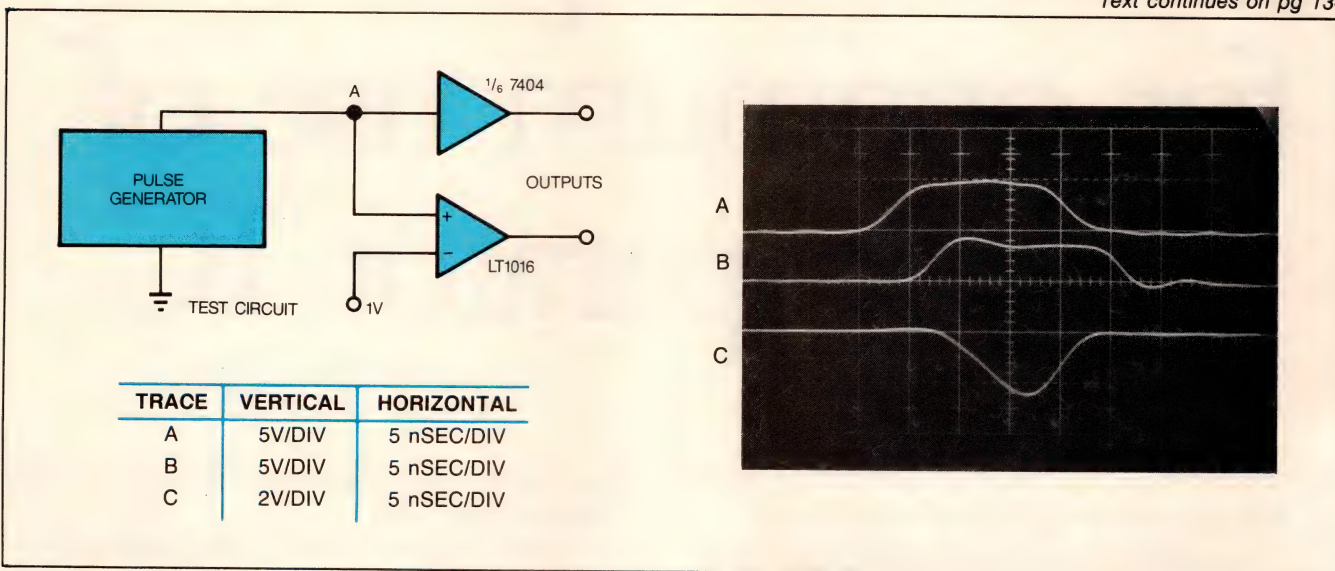


Fig 1—Faster than a TTL inverter, the LT1016 switches (trace B) in less than 10 nsec after application of an input pulse (trace A). The TTL circuit's output (trace C) never attains 0V.

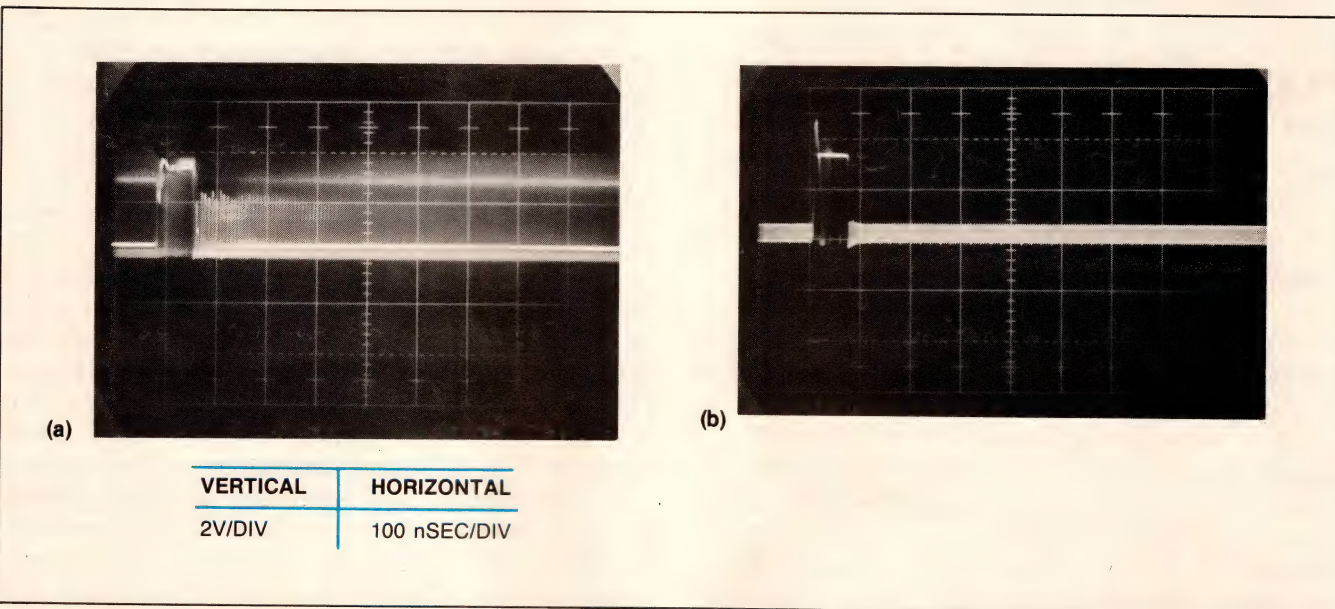


Fig 2—Proper bypassing is important, as shown by these scope photographs. The unbypassed case appears in a; b shows the result of inefficient bypassing (capacitors either too distant from the LT1016 or excessively lossy).

A fast TTL comparator

The LT1016 is a fast (10-nsec typ propagation delay) comparator that provides a direct interface to TTL logic while operating from either one 5V supply or dual $\pm 5V$ supplies. The IC offers matched complementary outputs and a latch pin for input-data retention at the outputs.

The LT1016's output stage provides active drive in both directions for high-speed drive into TTL logic or passive loads, yet does not exhibit the large current spikes usually found in totem-pole output stages. This attribute eliminates the need for a minimum slew-rate spec for the input signal, a spec that typ-

TABLE1—LT1016A KEY SPECIFICATIONS

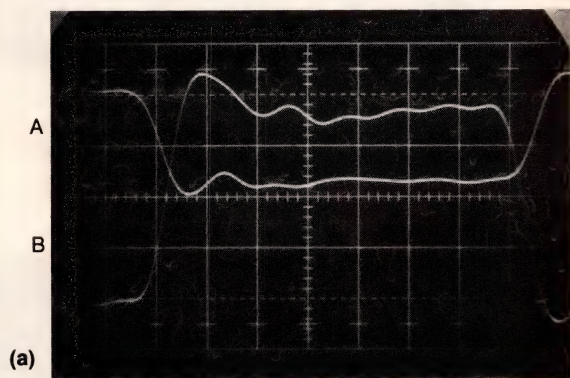
PARAMETER	SPEC
INPUT OFFSET VOLTAGE	1.5 mV MAX
OFFSET-VOLTAGE DRIFT	10 $\mu V/^{\circ}C$ MAX
INPUT BIAS CURRENT	10 μA MAX
INPUT-VOLTAGE RANGE	$V_{CC} - 1V$ $V_{EE} + 1.25V$
COMMON-MODE REJECTION	80 dB MIN
VOLTAGE GAIN	2000 MIN
PROPAGATION DELAY (5-mV OVERDRIVE)	12 nSEC MAX
V_{CC} CURRENT	35 mA MAX
V_{EE} CURRENT	5 mA MAX

ically encumbers other very fast comparators.

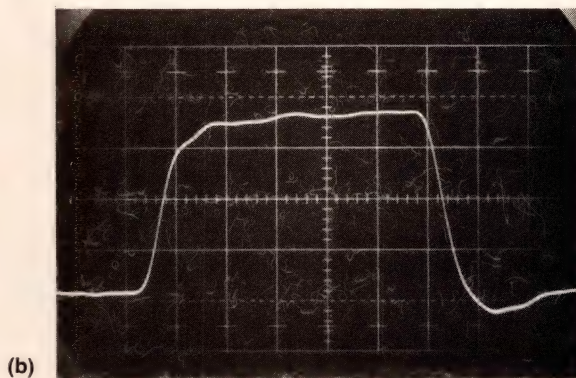
Another factor that makes the LT1016 easier to use than other

high-speed comparators is the fact that its outputs are stable when the device operates in its linear region, regardless of how slowly the input signal changes. This trait eliminates the problem of output chatter in the presence of slow-moving or dc-input signals.

Finally, the LT1016's quiescent negative-supply current is typically 2.5 mA—approximately 10 times lower than that of other very fast, bipolar comparators. This feature allows you to drive the negative-supply pin from any negative supply by using a simple resistive divider.



VERTICAL	HORIZONTAL
2V/DIV	10 nSEC/DIV



VERTICAL	HORIZONTAL
1V/DIV	50 nSEC/DIV

Fig 3—Proper selection and use of probes is all important. In a, a miscompensated probe yields a grossly exaggerated output (8V vs the true 5V); in b, an overcompensated (or insufficiently fast) probe delivers an unduly slow output to the oscilloscope.

Choose bypass-capacitor types and values with care

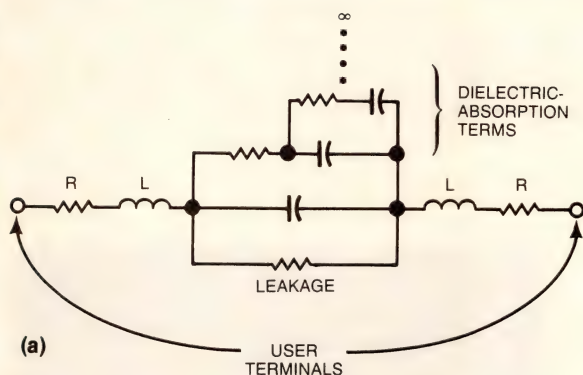
Bypass capacitors serve to maintain low power-supply impedance at the point of load. Because of parasitic resistance and inductance in supply lines, the supply impedance can often be very high. As frequency rises, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if you use local regulation, bypassing is still necessary because no power supply or regulator has zero output impedance at, say, 100 MHz.

The type of bypass capacitor to use is a function of the application, frequency domain of the circuit, cost, board space, and many other considerations. However, you can make some useful generalizations. All capacitors' equivalent circuits contain parasitic terms, some of which appear in **Fig Aa**.

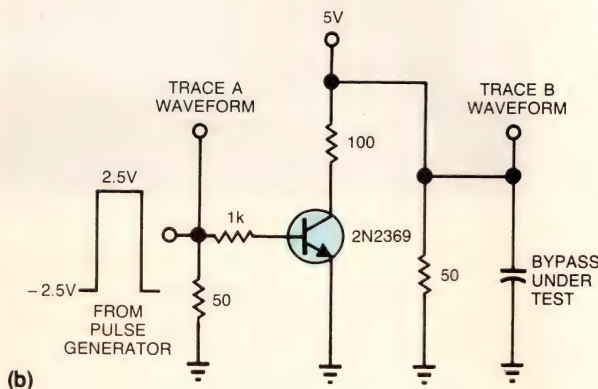
In bypass applications, leakage and dielectric absorption are secondary terms, but series inductance and resistance are not. These last two terms limit the

capacitor's ability to damp transients and to maintain low supply impedance. Bypass capacitors must often have large values so they can absorb long transients. In these cases, it's necessary to use electrolytic types, which exhibit high-value series inductance and resistance.

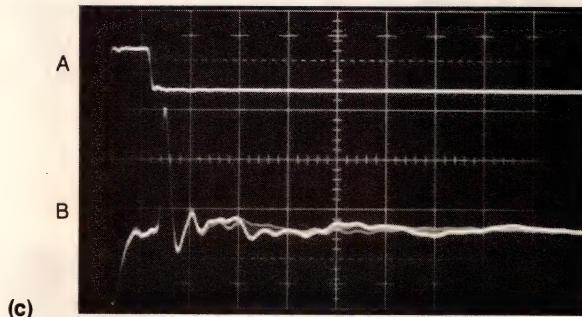
Different types of electrolytics—both polar and nonpolar—have markedly different characteristics, and the type (or types) to use is sometimes a subject of debate. In choosing a bypass ca-



(a)

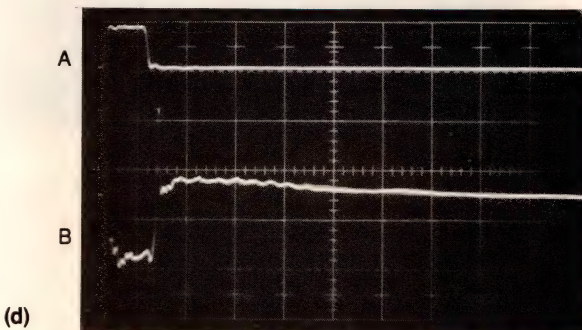


(b)



(c)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	1V/DIV	100 nSEC/DIV



(d)

Fig A—Understand the all-important bypass capacitors when you're designing high-speed circuitry. The diagram in **a** is the equivalent circuit of a capacitor. The important parasitics for bypassing are series inductance and resistance. The circuit in **b** allows you to test bypass capacitors. The scope photographs show the response with the various bypass combinations described.

capacitor, the test circuit in **b** and the accompanying scope photos can perhaps be useful. The photos show the response of five bypassing methods to the transient generated by the test circuit.

The photo in **c** shows an unbypassed line, whose voltage sags and ripples badly at high amplitudes. In **d**, a 10- μ F aluminum electrolytic cuts the disturbance considerably, but the potential for trouble still exists.

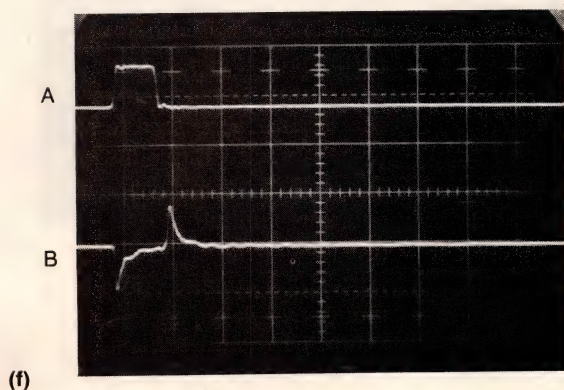
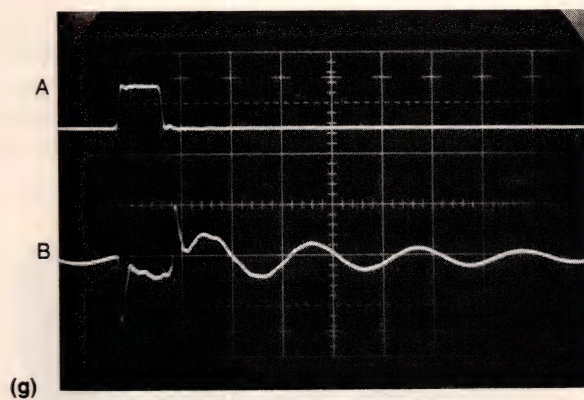
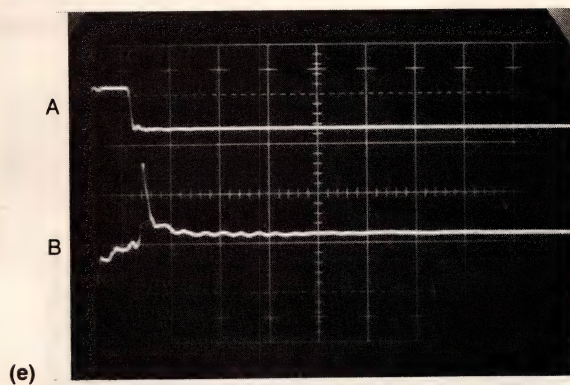
A 10- μ F tantalum unit (**e**) offers cleaner response; a 10- μ F

aluminum combined with a 0.01- μ F ceramic type (**f**) is even better. Combining electrolytics with other capacitor types (usually ceramic) is a popular way to obtain good response, but beware of picking the wrong duo.

Choosing the right pair is not an easy task. Circuit characteristics (including line inductance and the nature of the signals you're dealing with) and the capacitors' parasitic terms both play a role. The photo in **g**, for example, shows the results of

using a parallel combination of a 10- μ F aluminum electrolytic and a 0.1- μ F ceramic capacitor in the test circuit. Note the resonant, ringing response.

The preceding example shows that you must tailor bypass capacitors and capacitor combinations to your particular system. And this tailoring is more an empirical task than an analytical one. In other words, experiment with various bypass components in your system until you achieve the best results.



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	0.1V/DIV	100 nSEC/DIV

A high-speed IC needs a rock-stable and impedance-free supply to do its job properly. Therefore, supply bypassing is not only beneficial, but crucial.

internal characteristics of the devices connected to it. This fluctuation almost always causes unruly operation.

What's more, several devices connected to an unbypassed supply can effectively communicate through the finite supply impedances, thereby provoking erratic operating modes. Bypass capacitors, by providing local reservoirs of energy at the device level, represent a simple way to eliminate this communication. The bypass capacitor acts like an electrical flywheel that keeps supply impedances low at high frequencies. The choice of capacitor type for bypassing is a critical issue, so weigh your decision carefully (see **box**, "Choose bypass-capacitor types and values with care").

Fig 2a shows the response of an unbypassed LT1016 to a pulse input. The power supply that the comparator sees at its terminals has high impedance at high frequencies. This impedance forms a voltage divider with the LT1016, allowing the supply voltage to move in response to changes in the comparator's internal conditions. The supply instability causes local feedback, and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100-MHz oscillation.

In **Fig 2b**, the comparator's supplies are bypassed, but it still oscillates. This oscillation has two possible causes: The bypass units are either too far from the

LT1016, or they're lossy capacitors. These examples suggest two rules: *Use capacitors with good high-frequency characteristics, and mount them as closely as possible to the LT1016.* Even an inch of wire between the capacitor and the comparator can cause problems.

Perhaps number two in the list of circuit-environment problems is the use of improper—or the improper use of—oscilloscope probes. In **Fig 3a**, the comparator is properly bypassed, but a new problem arises. The photo shows both outputs of the comparator. Trace A appears normal, but trace B shows an excursion of almost 8V—quite a feat for a device running from one 5V supply. This anomaly is commonly reported in high-speed circuits, and it can be very confusing.

The anomaly arises from a grossly miscompensated or improperly selected oscilloscope probe. This example prompts another rule of thumb in working with high-speed circuitry: *Use probes that match your oscilloscope's input characteristics, and compensate the probes properly.* (For a further discussion of probes, see **box**, "Oscilloscopes and probes: Choose and use wisely.")

Fig 3b shows another probe-induced problem. Here, the amplitude seems correct, but the 10-nsec-response LT1016 exhibits 50-nsec edges. In this case, the probe

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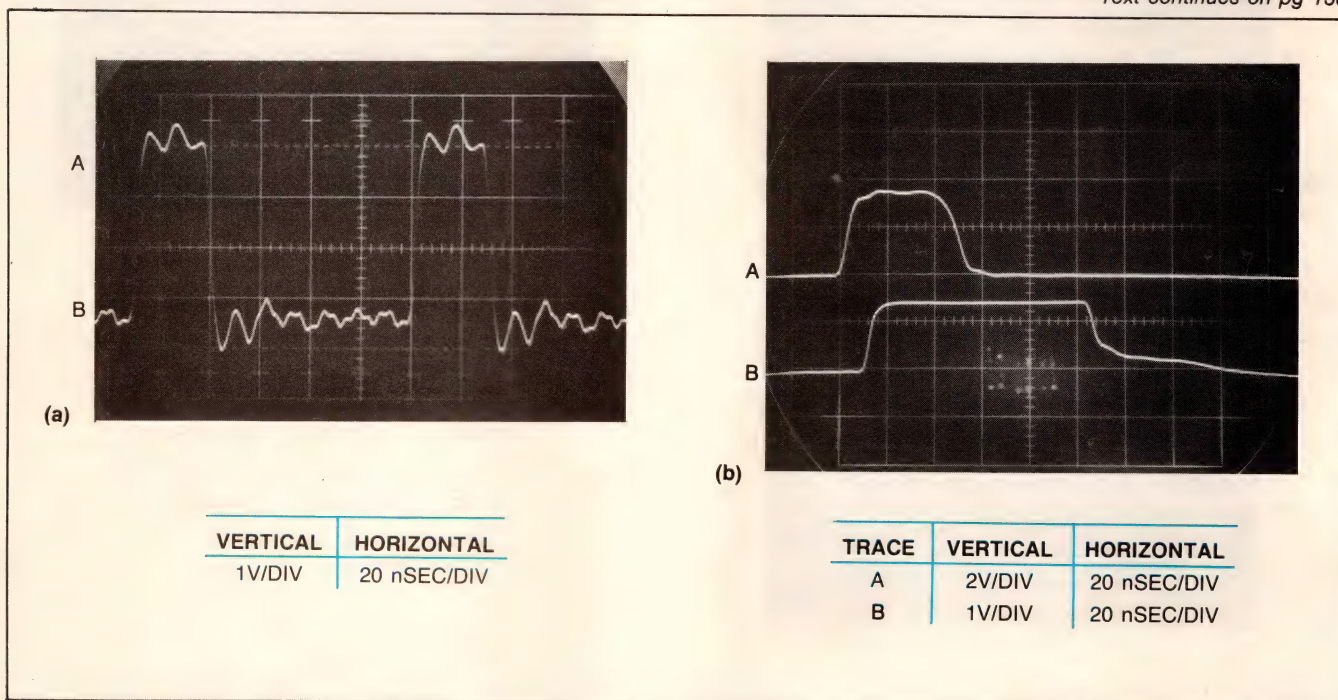


Fig 4—More probing-caused problems afflict these waveforms. In a, the probe's too-long ground lead causes ringing and distortion; in b, a badly overdriven FET probe delivers false information to the oscilloscope.

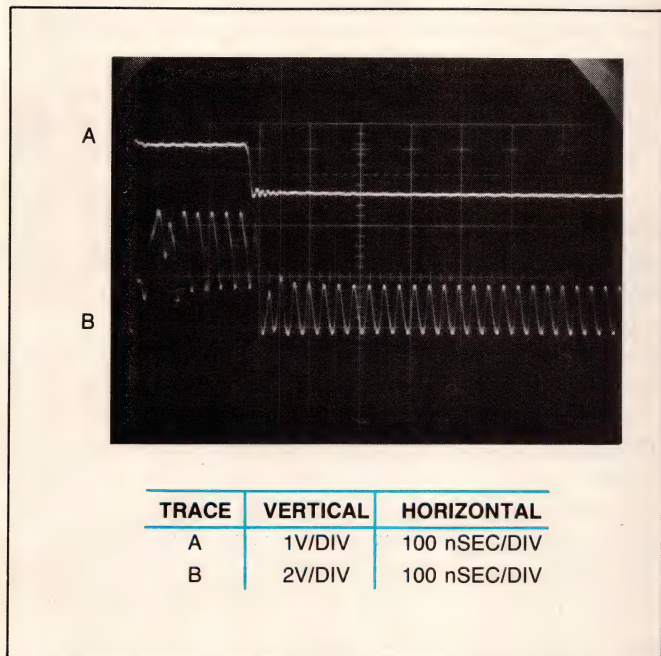


Fig 5—Improper grounding of high-speed ICs can lead to disaster. Trace B is the output of an LT1016 whose ground lead is 1 in. in length. The comparator oscillates at approximately 40 MHz. To avoid such problems, keep the IC's ground lead to less than $\frac{1}{4}$ in. in length.

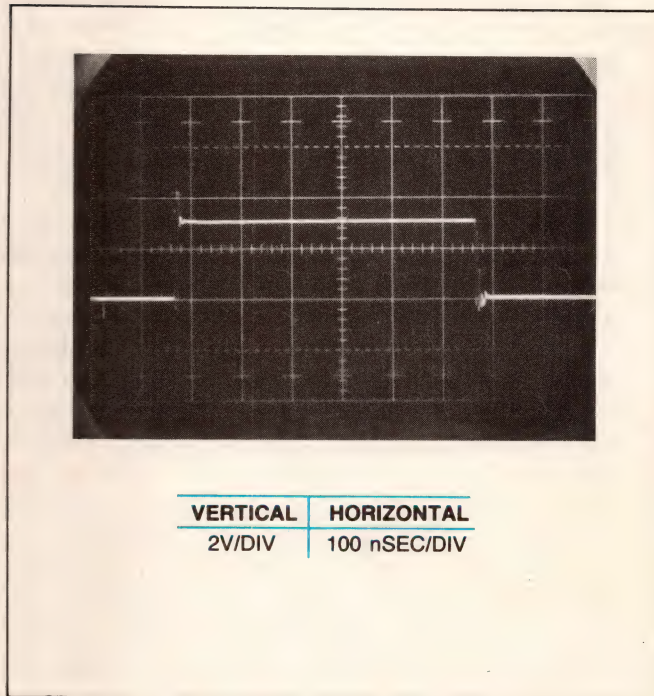


Fig 6—Failure to use a ground plane provokes the chattering edges on this waveform. A ground plane in this example would have reduced inductance sufficiently to eliminate the chatter.

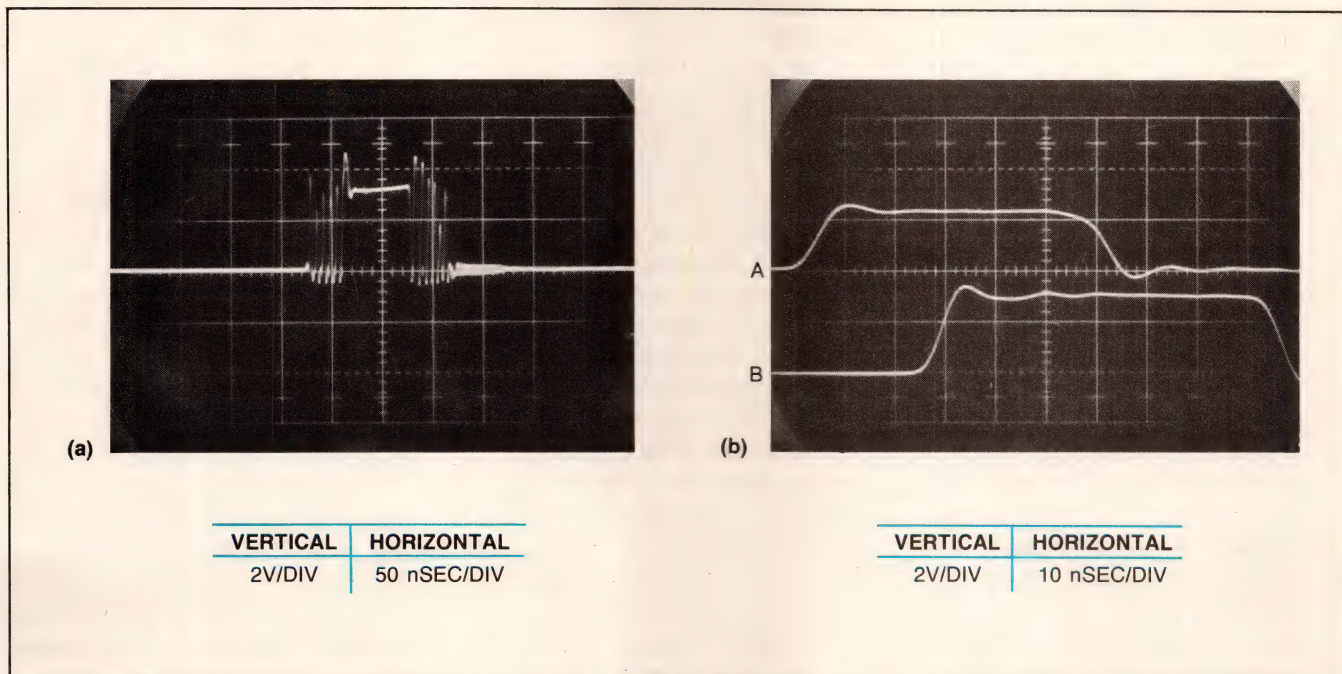


Fig 7—Stray capacitance from output to input causes the singing on the edges of the waveform in a. A lower source impedance at the comparator's input and some attention to input and output lead routing would cure this condition. More stray-capacitance-induced woes are evident in b, where the culprit is the stray capacitance to ground at the comparator's input.

Oscilloscopes and probes: Choose and use wisely

In high-speed-design work, the choice of an oscilloscope-probe combination is the most important decision you must make. Ideally, the oscilloscope should have at least 150-MHz bandwidth for work with the LT1016, but slower instruments are acceptable if you have a good understanding of their limitations. Be aware of your scope's behavior with respect to input impedance, noise, overdrive recovery, sweep nonlinearity, triggering, channel-to-channel feedthrough, and other characteristics.

Probes are the most overlooked cause of oscilloscope mis-measurement. All probes have some effect on the points they measure. The most obvious effect usually stems from the probe's input resistance, but input capacitance usually dominates in high-speed measurements. You can lose much time investigating circuit events that actually stem from improperly selected or applied probes.

An 8-pF probe observing a point with 1-k Ω source impedance, for example, will produce an 8-nsec lag—similar to the LT1016's response time. Low-impedance probes (with 50 Ω to 1-k Ω resistance) usually have input capacitance of 1 or 2 pF; these probes are a good choice if you can tolerate the low resistance.

FET probes maintain high input resistance and keep capacitance at the 1-pF level, but have substantially more delay than passive probes. FET probes also impose limitations on common-mode input range; you must respect the limits or serious measurement errors will occur. Contrary to popular belief, FET probes do not have *extremely* high input resistance—for some types, it's as low as 100 k Ω .

The passive, transformer-based types of current probes

are fast and they introduce less delay than the versions based on the Hall effect. The Hall-effect types, however, respond at dc and low frequencies, while the transformer-based probes typically roll off at approximately 100 to 1000 Hz. Both types have saturation limitations which, when exceeded, cause odd CRT-display results that can be confusing.

When using different probes, remember that each has a different delay time; therefore, apparent timing errors will occur on the oscilloscope screen. Know what the individual probe delays are, and account for them in interpreting the CRT display.

The greatest source of error by far in probe use is improper grounding. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases, the choice and placement of a probe's ground connection can affect waveforms on another channel. In the worst case, connecting a probe's ground wire can virtually disable the circuit you're measuring.

The cause of the cited problems is parasitic inductance in the probe's ground connection. In most oscilloscope measurements, the inductive effect is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in minimizing the inductance of the connection to ground. Most of these attachments assume a ground plane is in use (as it should be). Always try to make the shortest possible connection to ground—anything longer than 1 in. can cause trouble.

The simple network in **Fig Aa** shows just how easy it is for poorly chosen or improperly used probes to cause bad re-

sults. A 9-pF input-capacitance probe with a 4-in. ground strap monitors the output, seen in **b**, trace B. Although the input (trace A) is clean, the output contains ringing.

Using the same probe with a ¼-in. spring-tip ground-connection accessory seems to clean up everything (**c**). However, substituting a 1-pF FET probe (**d**) reveals a 50% amplitude error in **b**'s measurement. The FET probe's low input capacitance allows a more accurate display of the circuit's action.

The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5 nsec, owing to the delay in its active circuitry. Hence, you must make separate measurements with each probe to determine the amplitude and timing parameters of the output.

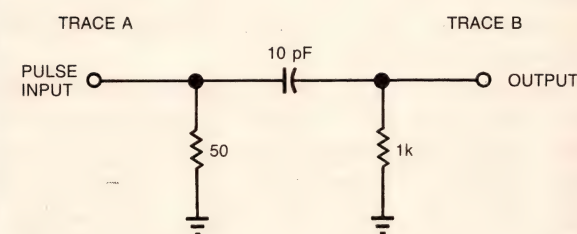
In **e**, probes A, B, E, and F are standard types equipped with various forms of low-impedance grounding attachments. The conventional ground lead used with probe G is the most convenient to work with, but causes ringing and other effects at high frequencies, thereby rendering the probe virtually useless.

Probe H has a very short ground lead. This lead is better, but can still cause trouble at high speeds. C is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. D is a separate FET-probe attenuator head. Such heads allow use of the probe at high voltage levels (eg, ± 10 or ± 100 V). You can mount the miniature coaxial connector on the circuit board, then mate the probe to it. The coaxial technique provides the lowest possible parasitic inductance; therefore, it's recommended.

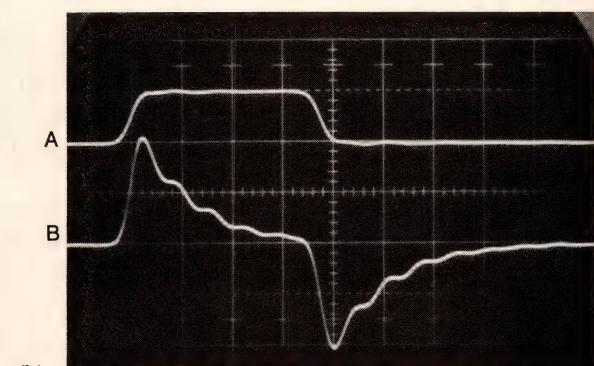
Probe I is a current probe; it usually doesn't require a ground connection. However, at high speeds, the ground connection might result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible.

A final form of probe is the human finger (J). Probing the circuit with a finger can accentuate desired or undesired effects, thereby giving clues to circuit behavior. You can use a finger, for example, to introduce stray capacitance into a suspect circuit node while observing results on

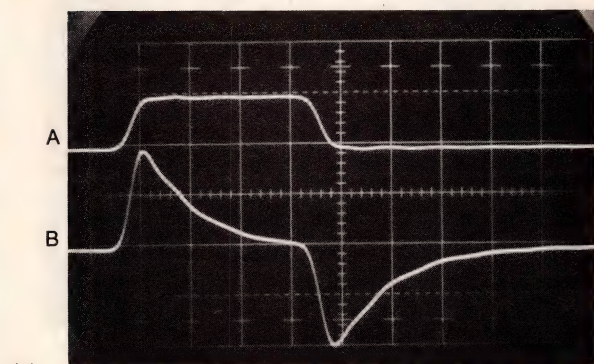
a CRT. You can use two fingers, lightly moistened, to provide an experimental resistance path. Some high-speed-circuit engineers are particularly adept at these techniques, and can estimate the simulated capacitive and resistive effects with surprising accuracy.



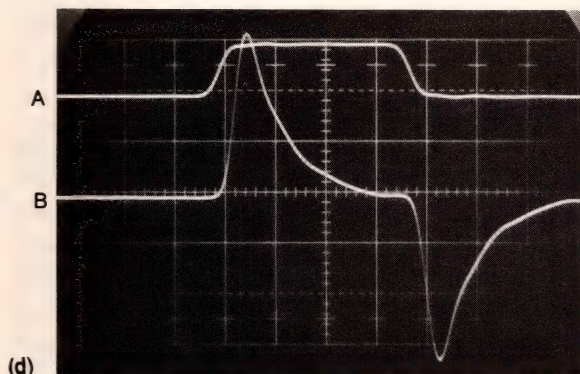
(a)



(b)

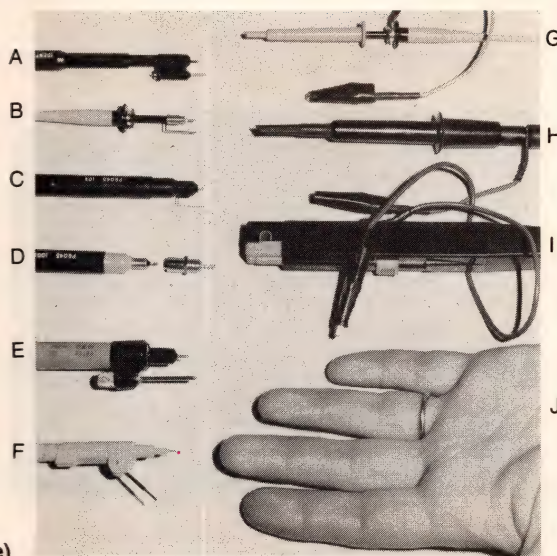


(c)



(d)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	1V/DIV	10 nSEC/DIV



(e)

Fig A—Choosing, and correctly using, appropriate probes is crucial in working with high-speed circuitry. The test network in a serves as an evaluation vehicle for various probes. In b, the probe's long ground lead causes ringing. A shorter ground strap (c) cleans up the ringing, but the FET probe's low input capacitance shows in d that the previous probe's high capacitance led to amplitude errors. Various types of probes and ground attachments are shown in e.

A prevalent cause of measurement problems, the improper choice or use of scope probes can lead to misleading or false results when testing high-speed circuitry.

used is too heavily compensated or too slow for the oscilloscope. Never use, for example, 1X (unattenuated) probes. Their bandwidth is 10 to 20 MHz or less, and their capacitive loading is high. The rules: *Check probe bandwidth to ensure that it's adequate for the measurement. Equally important, use an oscilloscope with adequate bandwidth.*

Additional probe problems

Limited bandwidth and capacitive loading are not the only sources of probe-induced woes. In **Fig 4a**, the probes are properly selected and compensated, but the LT1016's output rings and distorts badly. In this case, the probe's ground lead is too long. For general-purpose work, most probes use ground leads about 6 in. long. At low frequencies, this length is fine—at high frequencies, however, the long ground lead takes the form of an inductor, and the illustrated ringing occurs.

High-performance probes are always supplied with some short ground straps to deal with the problem. Some come with very short spring clips that mate directly with the probe tip to facilitate a low-impedance ground connection. For high-speed work, the ground connection to the probe should not exceed 2 in. in length. *Keep the probe's ground connection as short as possible.*

A final probe-induced problem causes the aberrations of **Fig 4b**. The problems in trace B are delays and insufficient amplitude. A small delay on the leading edge is followed by a long delay before the falling edge begins. In addition, a lengthy, tailing response stretches to 70 nsec before finally settling. The amplitude rises to only 1.5V. A common oversight in probing is responsible for these conditions.

In this example, a FET probe monitors the LT1016's output. The comparator's output greatly exceeds the probe's common-mode input range, thereby causing the probe to overload and clip badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the LT1016's output is high, the probe is driven deeply into saturation. When the output drops, the probe's recovery is lengthy and uneven, causing the delay and long tail.

Thus, some final probe-related rules: *Know your FET probe. Take account of the delay of its active circuitry. Avoid saturation effects arising from common-mode input limitations (typically $\pm 1V$). Use 10X and 100X attenuator heads when required.*

Fully as important as—and closely related to—the bypassing issue, proper grounding is crucial in any high-frequency application of the LT1016 (or any other high-speed IC). **Fig 5**, for example, shows the LT1016's

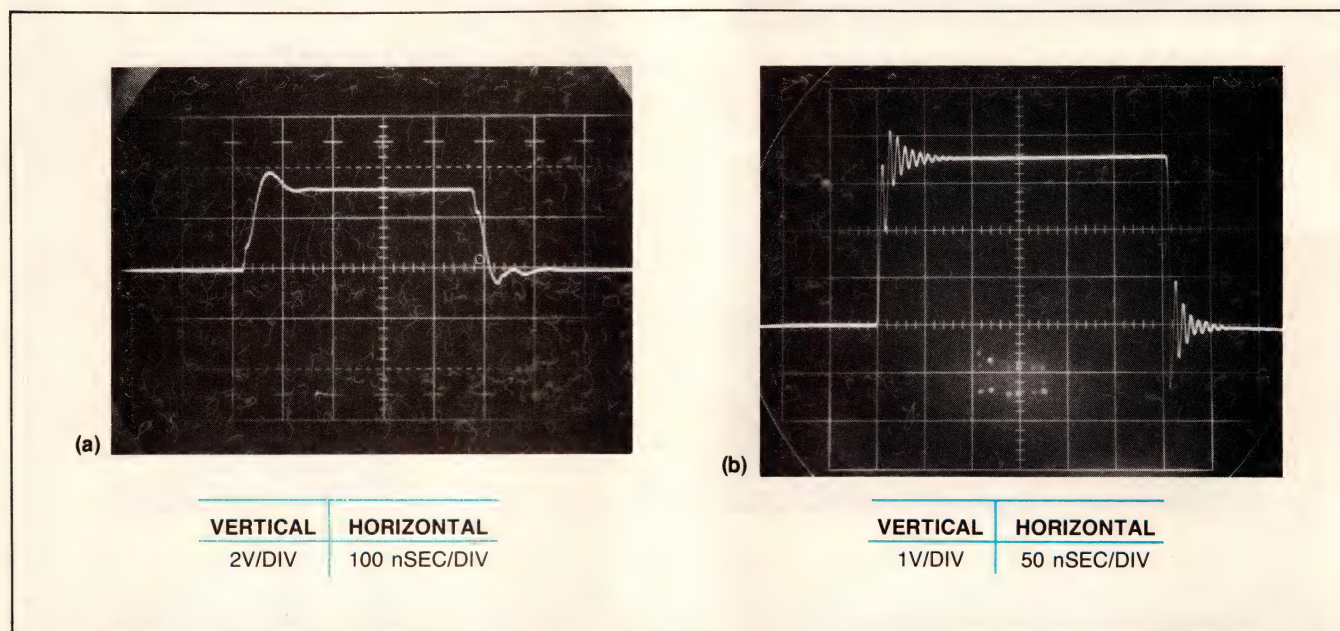


Fig 8—Beware of output-loading problems in using the LT1016. In **a**, a large capacitive load causes distortion and slow response on the output's edges. For heavy capacitive loads, use a buffer. In **b**, the LT1016 faces a load that resembles an unterminated transmission line. The solution is to terminate the line with a resistor, or to shorten the output-lead length.

output (trace B) oscillating at approximately 40 MHz as it responds to an input (trace A). Note that the input signal shows traces of the oscillation. The problem in this example is improper grounding of the comparator. In this case, the LT1016's ground-terminal connection is 1 in. long.

The ground lead of the LT1016 must be as short as

possible, and it must be connected directly to a low-impedance ground point. Any substantial impedance in the comparator's ground path will generate effects like those shown in Fig 5. The source of the malady is related to the necessity for bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, thereby caus-

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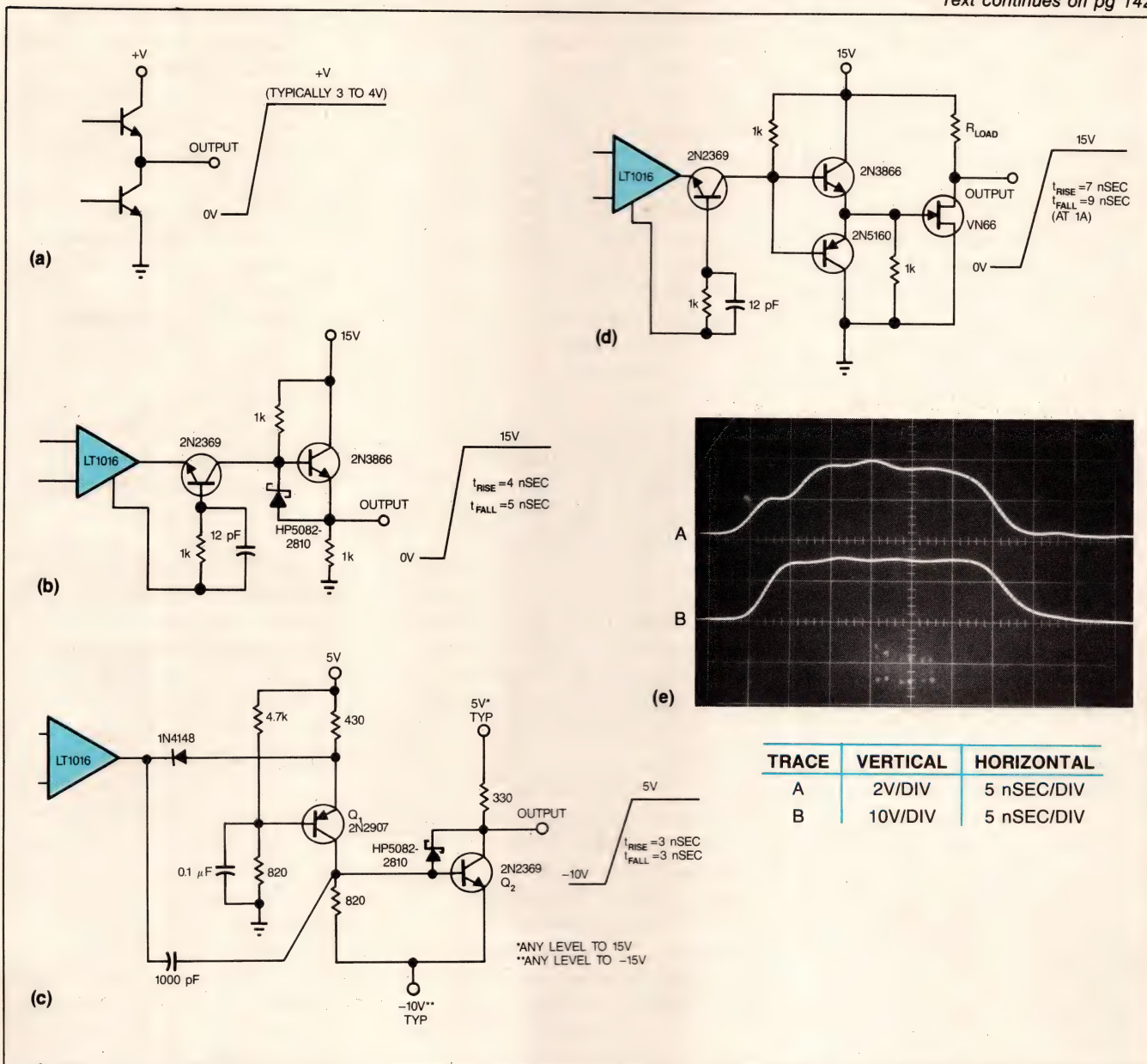


Fig 9—Level shifting is not a trivial task. These level-shifting circuits take advantage of the LT1016's sink-source output (a) to provide shifting with very small delays. The shifters suit various applications. The circuit in b, for example, provides a 15V unipolar output. The configuration in c allows you to vary the levels; e shows waveforms for this circuit. The setup in d provides a 15V, 1A output.

Understand the rules for ground planes

The term "ground plane" crops up frequently in discussions of high-frequency circuit layout, most often as a mystical and ill-defined cure for spurious circuit operation. In fact, there is little mystery surrounding the usefulness and operation of a ground plane, and—like so many phenomena—its fundamental operating principles are surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance; they do so in accordance with basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and the distance from the conductor.

You can thus visualize a current-carrying wire (**Fig Aa**) surrounded by magnetic-field lines. The unbounded field diminishes with distance from the wire. A wire's inductance is defined as the energy stored in the field set up by the wire's current. Computing the inductance requires integrating the field over the wire's length and the total radial area of the field.

The inductance calculation implies integrating the magnetic field on the radial line from the wire's radius to infinity. However, consider **Fig Ab**, in which two parallel wires in space carry the same current in opposite directions. The fields essentially cancel, and the inductance in this case is much lower than in the case of the single wire. You can make this inductance arbitrarily small by reducing the dis-

tance between the two wires.

The reduction of inductance between current-carrying conductors is the underlying operating principle of ground planes. In a normal circuit, the path that a current takes from its signal source, through a conductor, then back to ground includes a large loop area. The loop area gives rise to a high inductance for the conductor, thereby producing ringing because of tank-circuit effects. It's worth noting that 10 nH at 100 MHz has an impedance of 6.3Ω , so a mere 10 mA produces a 63-mV drop.

A ground plane provides a return path directly under the signal-carrying conductor, a path through which return currents can flow. Thanks to the small separation of the conductors, the inductance is low. The return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor.

In a practical circuit, it's desirable to make a ground plane of one entire side of the pc card—usually the component side, for wave-soldering considerations—and run the signal conductors on the other side. This technique provides a low-impedance path for all return currents.

There are some practical hints about ground planes.

- On the component side of the board, devote as much

area as possible to a ground plane (especially under traces that operate at high frequencies).

- Mount components that conduct substantial fast-changing currents as closely as possible to the board. Such items include termination resistors, ICs, transistors, and decoupling capacitors.
- Where common ground potential is important (eg, at comparator inputs), try to ground the components at one point on the ground plane, thereby avoiding ac drops.
- Keep trace lengths short. Inductance varies directly with length, and no ground plane provides perfect cancellation.

In the circuit in **c**, for example, good practice dictates that, insofar as possible, grounds 2, 3, 4, and 5 connect to one point. Fast-changing, large currents must flow through R_1 , R_2 , D_1 , and D_2 during the D/A converter's settling time. You should thus mount these components close to the ground plane, thereby minimizing their inductance.

R_3 and C_1 carry no current, so their inductance is of minor importance. You could insert them vertically to save space and to allow point 4 to more easily share a single-point ground with points 2, 3, and 5. In critical circuits, you must often trade the beneficial effects of lowered inductance for the loss of a single-point ground.

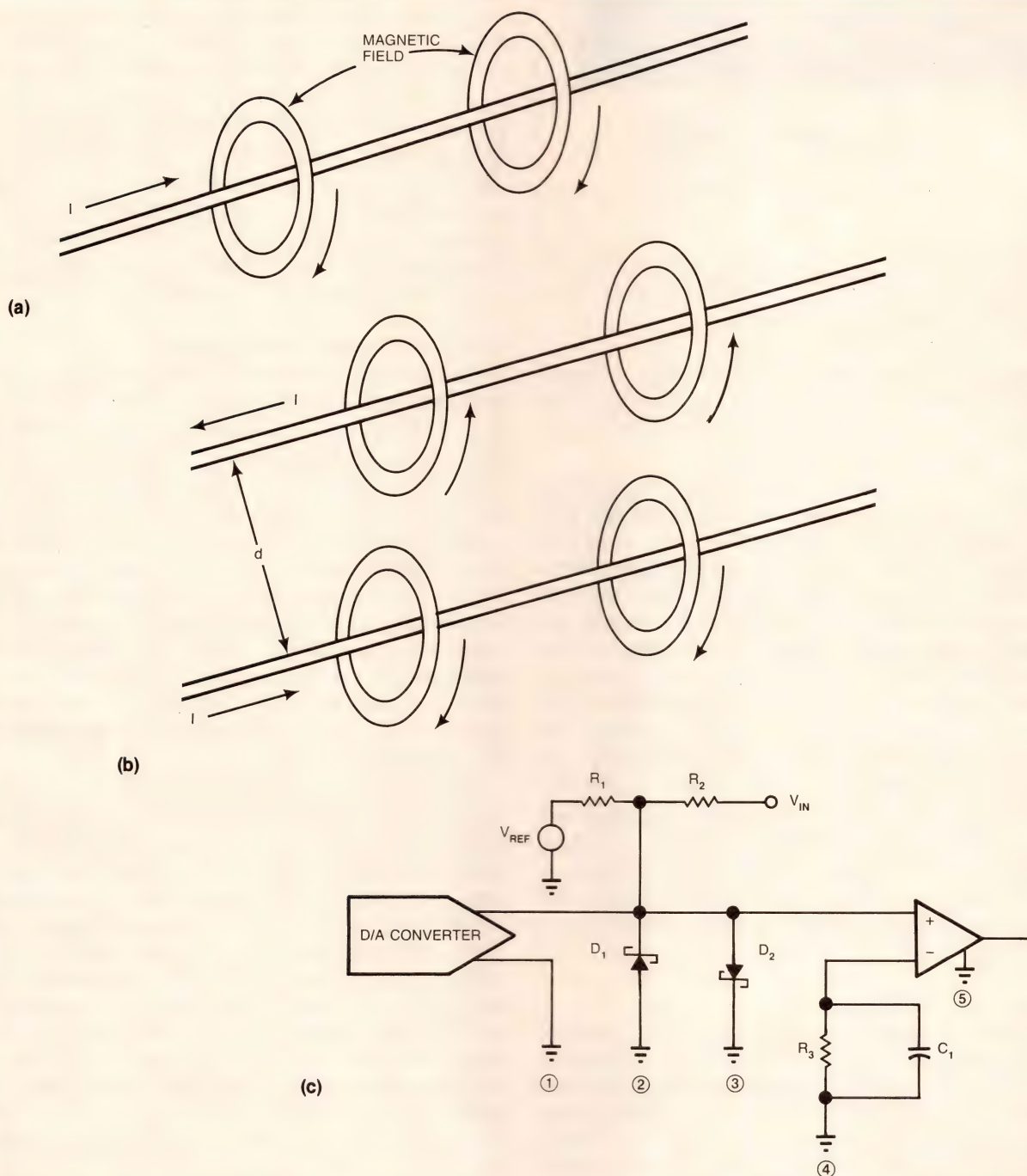


Fig A—Not a convenience, but a necessity: Ground planes are essential in high-speed circuitry. They minimize inductance by cancelling the magnetic fields generated by currents in conductors. The diagrams in **a** and **b** show the fields and cancellation thereof. In the circuit example in **c**, it's important to provide a single-point ground for the components carrying fast-switching currents.

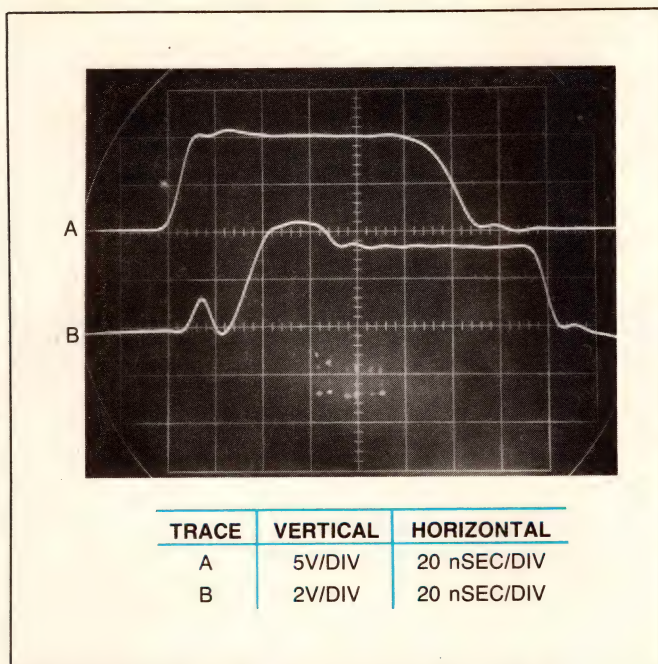


Fig 10—Grossly overdriving the LT1016's inputs can result in output aberrations, as seen in trace B. Keep common-mode input voltages within spec-sheet limits at all times.

ing undesired effects in the IC. The fix here is simple: *Keep the LT1016's ground connection as short as possible (typically ¼ in.), and run it directly to a low-impedance ground. Do not use sockets.*

To further illustrate the importance of using a low-impedance ground, **Fig 6** shows the effects of failing to use one. In this example, the output is clean except for chattering around the rising and falling edges. Here, the LT1016 operates without a ground plane (see **box**, "Understand the rules for ground planes"). You form a ground plane by placing a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuits' necessary current paths.

The ground plane serves two functions. Because it's flat (ac currents travel along the surface of a conductor) and covers the entire area of the board, it provides access to a low-inductance ground point from anywhere on the board. Second, it minimizes the effects of stray capacitance in the circuit by referring the strays to ground. This stray neutralization breaks up unintended and harmful feedback paths. In short, *always use a ground plane with the LT1016.*

Effects of stray capacitance

The stray capacitance mentioned in the previous section can produce undesirable effects in comparator performance. Consider, for example, the fuzzy edges of the output waveform in **Fig 7a**. This condition appears similar to that of **Fig 6**, but the oscillation is more stubborn and persists well after the output switches low. The cause is stray capacitance from the comparator's outputs to its inputs. A 3-k Ω input-source impedance and 3-pF stray-capacitance feedback allowed this oscillation. The solution for this condition is not difficult: *Keep source impedances as low as possible (pref-*

As the operating speed of circuits increases, proper grounding becomes more important. It's crucial to minimize series inductance and resistance.

erably ≤ 1 k Ω). Route output and input pins and components away from each other.

The opposite of stray-induced oscillations appears in **Fig 7b**. Here, the output response (trace B) badly lags the input (trace A). The lag arises from some combination of high source impedance and stray capacitance to ground at the input. The resulting RC network forces a lagging response at the input, resulting in an output delay. An RC combination of 2-k Ω source resistance and 5-pF capacitance to ground yields a 10-nsec time constant—the same as the LT1016's response time. Thus, *keep source impedances low and minimize stray capacitance from input to ground.*

Avoid heavy capacitive loading

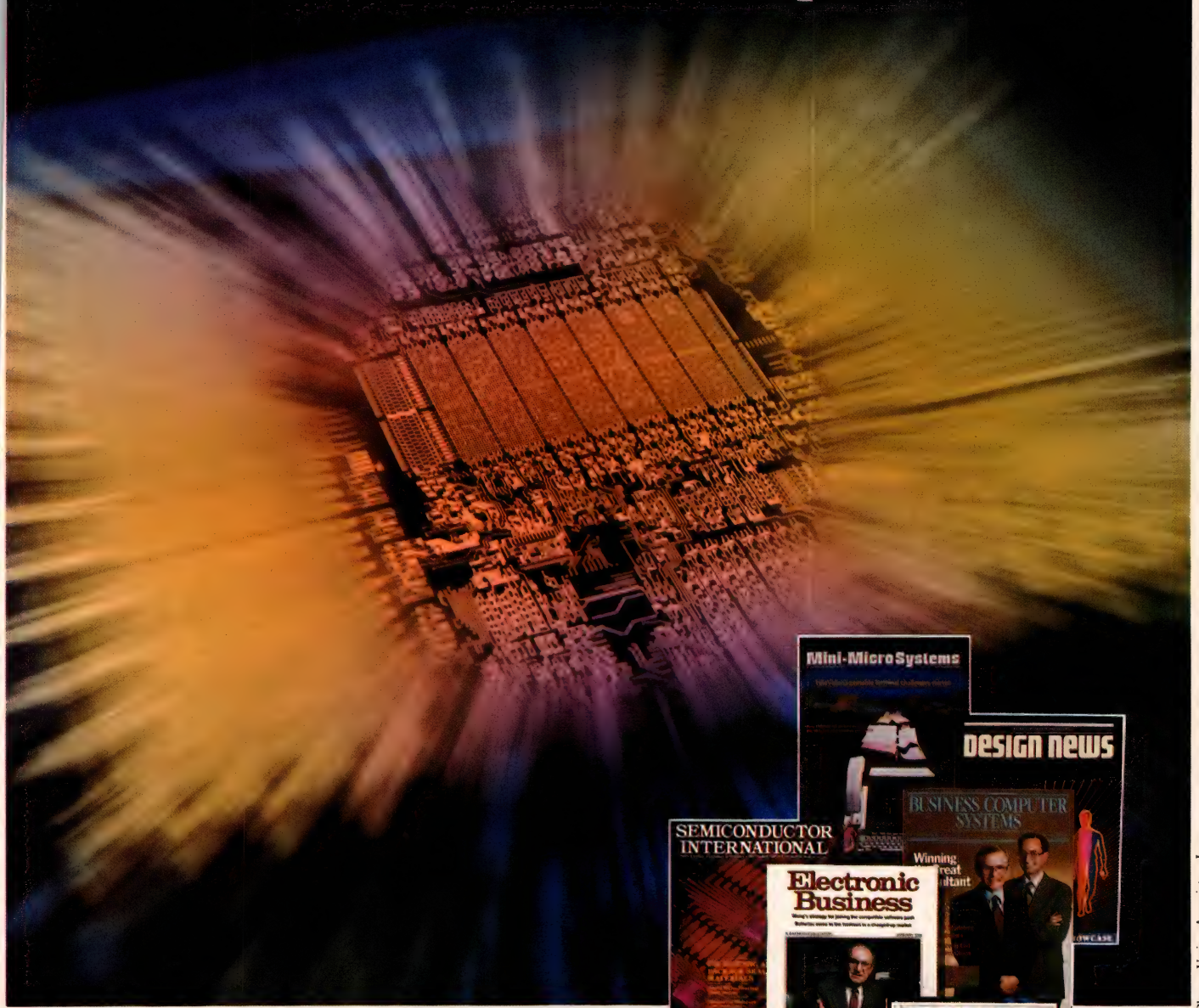
Feedback and shunt strays are not the only capacitive offenders in a high-speed comparator's erratic operation. **Fig 8a** shows another capacitance-induced problem. Here, the output does not oscillate, but its transitions are discontinuous and relatively slow. The problem is a large output-load capacitance. Its genesis could be a cable, excessive output-lead length, or the input characteristics of the circuit following the LT1016. In most situations, heavy capacitive loading is undesirable; you can eliminate it by using a buffer stage. In a few circumstances, the loading might not affect overall circuit operation. *Consider the comparator's output-load characteristics and their potential effects on the circuit. If necessary, add a buffer between the output and the load.*

Another output-caused fault is shown in **Fig 8b**. The output transitions are initially clean but end in ringing. The key to the solution here is the ringing. The phenomenon arises because of an output lead that's too long. The lead, which appears as an unterminated transmission line at high frequencies, causes reflections. The transmission-line effect accounts for the ringing and the abrupt reversal of direction on the leading edge. When the comparator drives normal TTL circuits, the aberration might be acceptable; other loads, however, might not tolerate it. The direction reversal, for example, could cause trouble with a high-speed TTL load. The rule: *Keep output lead lengths short. When they're longer than a few inches, terminate the line with a resistor (typically between 200 and 500 Ω).*

Another aspect of the LT1016's TTL outputs is that you must sometimes shift the levels of the output-voltage swing. In LT1016-based circuits, this task is not trivial; it's necessary to maintain very low delays in the

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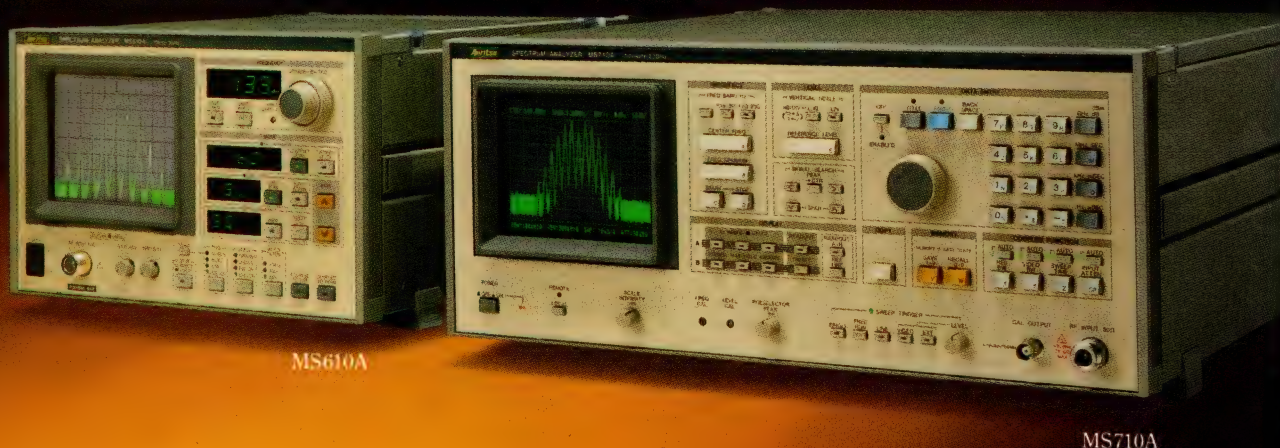
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Beware of such stray-reactance problems as feedback or shunt capacitance and series inductance. Such unwanted circuit terms can cause ringing, oscillation, or worse.

level-shifting stage to obtain optimum performance. When you design level shifters, keep in mind that the comparator's output stage is a sink-source pair (Fig 9a) with a reasonable ability to drive capacitance (eg, feed-forward capacitors).

Fig 9b shows a noninverting voltage-gain stage with a 15V output. When the LT1016 switches, the 2N2369's base-emitter voltage reverses, causing the transistor to switch very rapidly. The 2N3866 emitter follower affords a low-impedance output; the Schottky diode aids the circuit's current-sinking capability. Fig 9c shows a very versatile stage. It offers a bipolar swing whose levels you can program by varying the output transistor's supplies.

The 3-nsec stage is ideal for driving FET-switch gates. Q_1 , a gated current source, switches the Baker-clamped output transistor, Q_2 . The heavy feed-forward capacitor from the LT1016 is the key to low delays; it

provides Q_2 's base with nearly ideal drive. This capacitor loads the LT1016's output (Fig 9e, trace A), but Q_2 's switching is clean (trace B) and exhibits 3-nsec delay in its rising and falling edges.

The circuit in Fig 9d is similar to that in Fig 9b, except that a sink transistor replaces the Schottky diode. The two emitter followers drive a power MOSFET that switches 1A at 15V. Most of the 7- to 9-nsec delay in this stage occurs in the MOSFET and the 2N2369. When designing level shifters, remember to use transistors with high switching speeds and high f_T s. To obtain results like the ones in these examples, you'll need switching times in the 2-nsec range and f_T s approaching 1 GHz.

A final example of environment-induced maladies is shown in Fig 10. These waveforms are reminiscent of the input-RC-induced delay of Fig 7b. The output waveform initially responds to the input's leading edge,

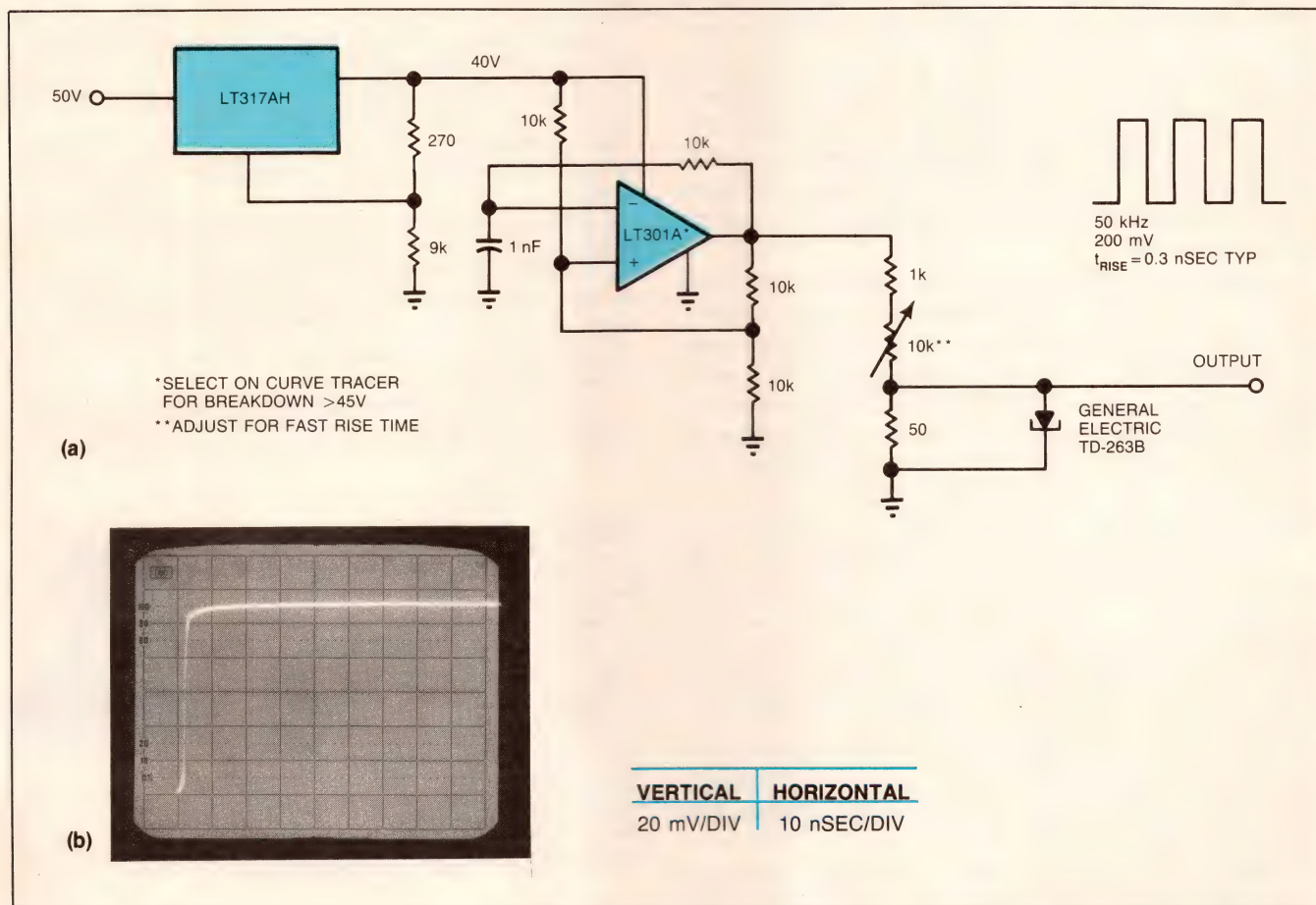


Fig 11—Be sure of your input pulses when measuring the response of your equipment. The circuit in a uses a tunnel diode to generate very clean pulses with rise times much lower than 1 nsec (b).

Respect a high-speed comparator's data sheet with regard to such parameters as common-mode input range and capacitive-load ability.

but then returns to zero before switching high again. When it does switch high, it slews slowly. Other odd characteristics include pronounced overshoot and pulse-top aberration. The fall time is also slow, and it's well delayed from the input. This behavior is certainly unusual for a TTL output.

All of these TTL-output anomalies are caused by the input pulse. Its 10V amplitude is well outside the 5V-powered LT1016's common-mode input range. Internal input clamps prevent such a pulse from damaging the comparator, but an overdrive of this magnitude invariably results in poor response. *Keep input signals within the LT1016's common-mode input range at all times.*

Verify equipment response

Although some of the examples described earlier dealt with probe-caused problems, oscilloscopes, too, can be troublesome. Your choice of oscilloscope is crucial. Be certain of the characteristics of the probe-oscilloscope combination you're using. You must take account of rise time, bandwidth, resistive and capacitive loading, delay, overdrive recovery, and other limitations. High-speed linear circuitry demands a great deal from test equipment; you can save countless hours if you're familiar with the characteristics of the instruments you use.

For example, the 10-nsec response of the LT1016 and the circuitry it's used in challenge the best test equipment. Many of the measurements you must make push equipment to the limits of its capabilities. It's a good idea to verify such attributes as probe and scope rise time and differences in delays between probes and even oscilloscope channels. To effect such verification, you need a source of very fast, clean pulses.

The circuit shown in Fig 11a uses a tunnel diode to generate a pulse with a rise time well under 1 nsec. Fig 11b shows that the pulse is clean, with no attendant ringing or noise. In the photograph, the pulse serves to check a probe-scope combination whose specified rise time is 1.4 nsec. The display shows that the equipment is being used properly and is within specification. By using the tunnel-diode generator to perform such tests, you can save countless hours pursuing supposed circuit problems, which in reality arise through misapplied or out-of-spec equipment.

You can, in fact, obtain good results with seemingly inadequate equipment if you know and respect the equipment's limitations. All the applications to appear in the two follow-on articles involve rise times and

delays that correspond to frequencies that are greater than 100 or 200 MHz, but 90% of the development work was accomplished with a 50-MHz oscilloscope. Familiarity with equipment and thoughtful measurement techniques permit useful measurements that are seemingly beyond instrument capabilities.

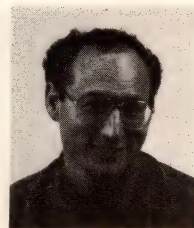
A 50-MHz oscilloscope, for example, cannot track a 5-nsec rise-time pulse, but it can measure a 2-nsec delay between two such events. Using such techniques, you can often deduce the desired information. There are situations, though, where no amount of cleverness will work, and you must use the right equipment (eg, a faster oscilloscope). In general, *use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything on the oscilloscope makes sense.* **EDN**

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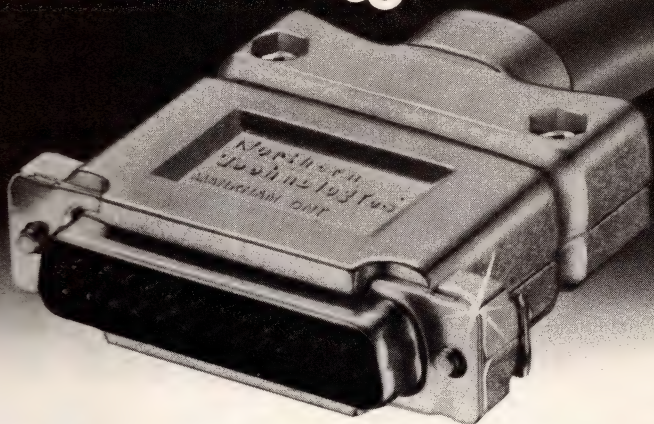
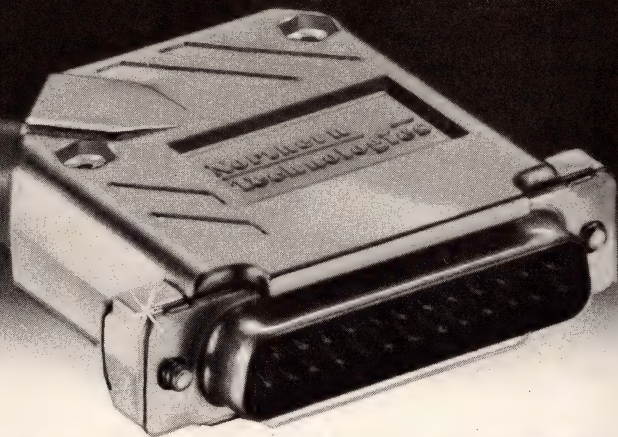
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Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.



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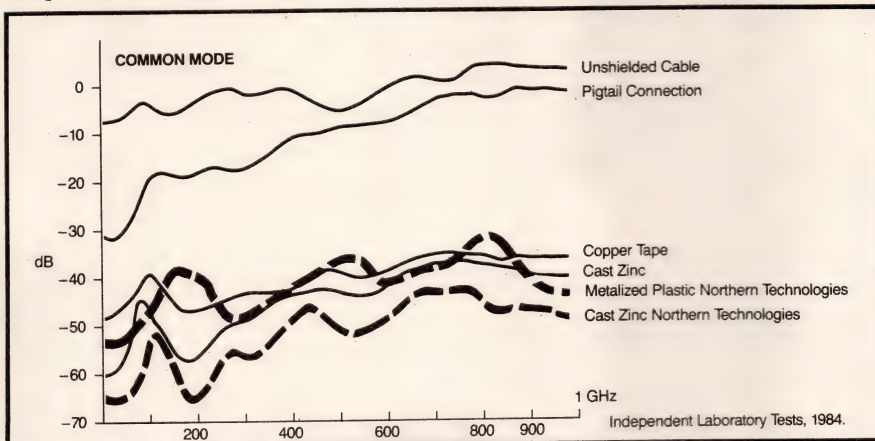
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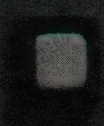
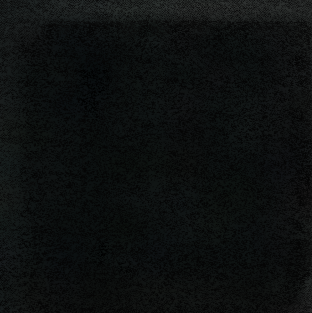
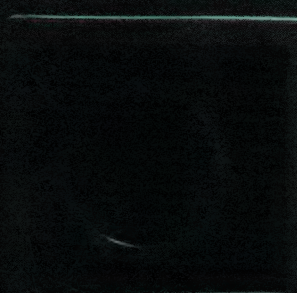
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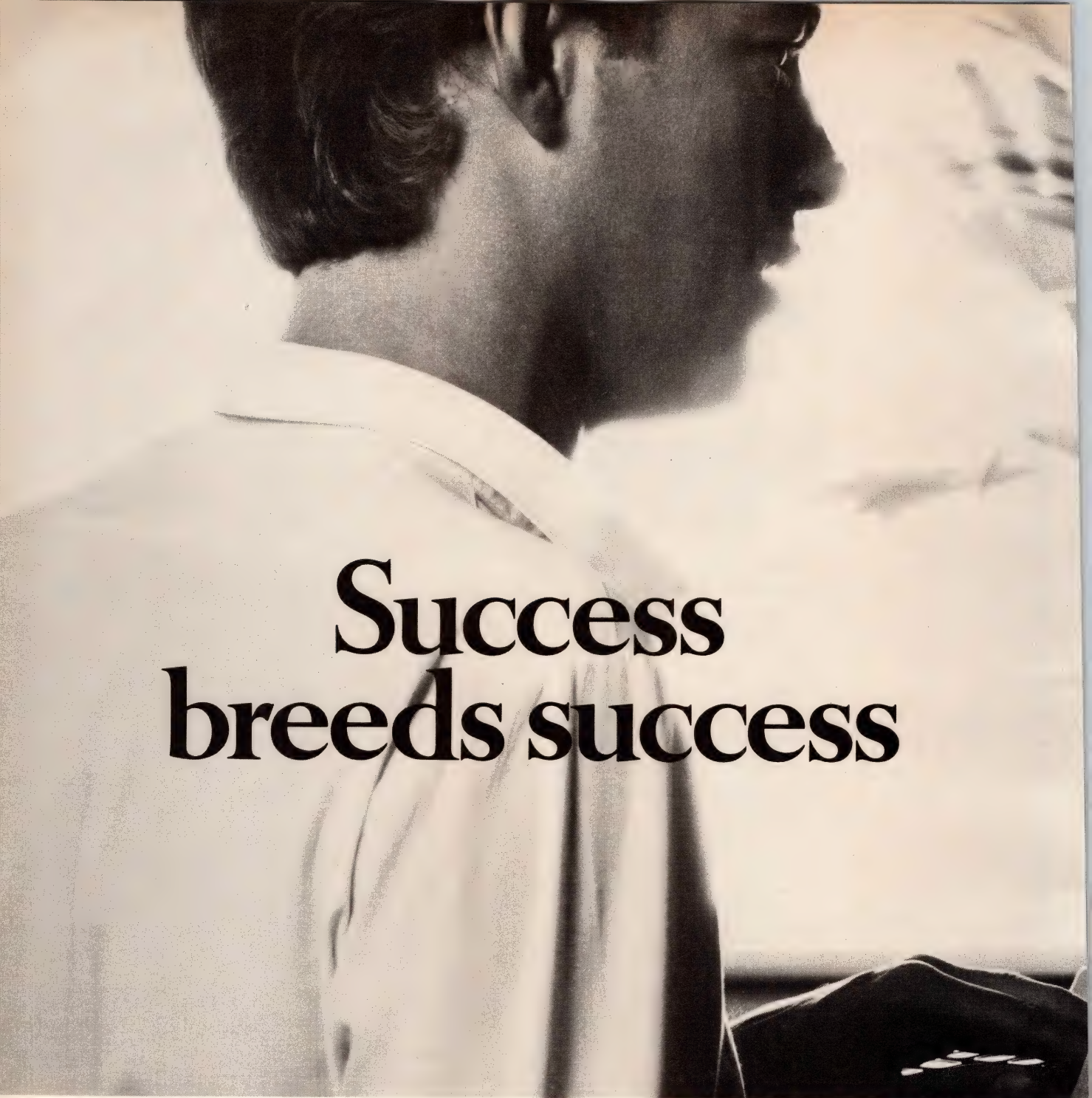
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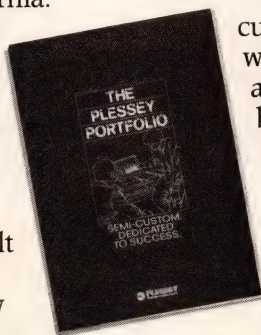
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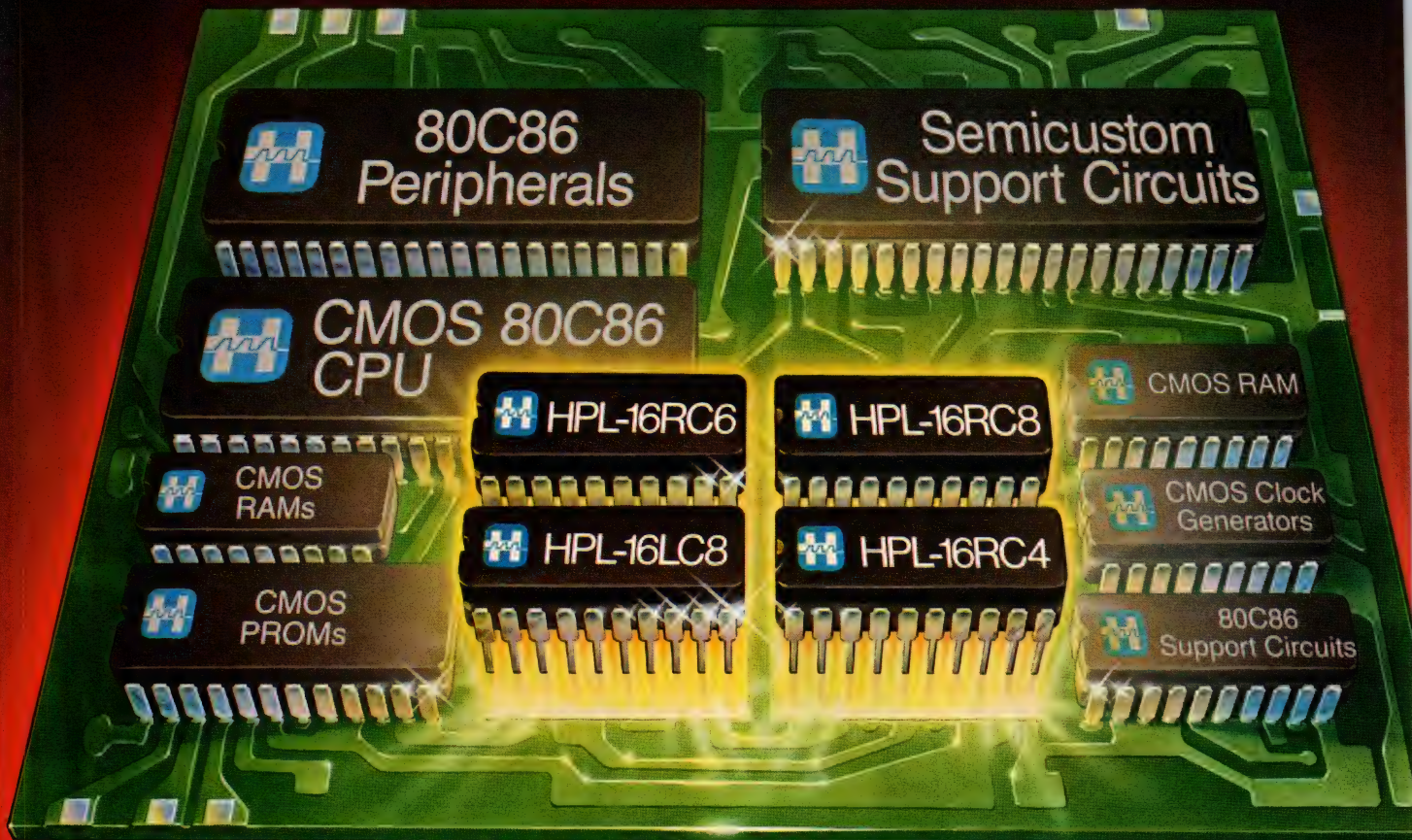
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CIRCLE NO 68

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CIRCLE NO 69

Input vectors drive simulation of logic-array designs

To evaluate logic-array designs correctly, logic simulators require accurate input vectors. You must generate the appropriate vectors to verify your logic's functionality and to determine dynamic operation, performance margins, and critical timing constraints like setup and hold times.

Michael Franz, Applied Micro Circuits Corp

In logic-array design, the input signals are as important to determining the behavior of the circuit as the logic diagram is. These input signals, when used as simulation vectors and test vectors during the design phase, serve as a design specification and as a means of verifying and testing a design. Consequently, they must be as correct as the logic design before you can be confident that your physical implementation operates as intended.

This article is the first of a 2-part series for designers who are beginning to use logic simulators and automatic test equipment (ATE) for the design and testing of logic arrays. This installment discusses logic-array requirements for input vectors to logic simulators, requirements that are similar to those for pc-board-level designs. Part 2 (scheduled for EDN's June 27 issue) will

examine issues of logic-array testing and the generation of correct test vectors, using functional simulation vectors as a starting vector set.

Simulation vectors allow you to establish the functional and timing integrity of a design. They drive a circuit through all intended logic functions, at or above the specified clock or data rate, to verify that it's functionally and dynamically in agreement with the designer's intentions. The primary tool for functional and timing verification is the logic simulator, a program that runs on an engineering workstation or mainframe computer.

In contrast, test vectors are used to verify that a chip is free of defects. The dynamic stimulation of a circuit by a tester is subject to constraints that don't affect a logic simulator. Testers have a limited test frequency that's slower than the operating speeds of many systems and chips. Also, inputs to the circuit being tested inevitably experience skew that can be attributed to pin-electronic drift and differences in the signal paths to the device under test. Finally, completeness of test vectors is important, because the primary objective for the design of test vectors is high fault coverage rather than functional verification.

Simulator needs net list for vectors

To examine the performance of a logic design, the logic simulator first needs a description of the design and then a set of input signals, collectively called input vectors, that describe how the environment outside the

To evaluate a circuit's function, a logic simulator needs both a circuit description and a set of input signals emulating the circuit's environment.

design stimulates the logic. On the simulator's computer, you generate the description of the design, called a net list, using building blocks that the simulator can interpret. The blocks are either simple logic units (such as 2-input NOR gates), which are directly understood by the simulator, or hierarchical constructs thereof, which are stored in software libraries. For logic arrays, these building blocks are called macros, and the hierarchical constructions are called structural models because they describe the internal structure of a particular circuit function.

Advanced logic simulators also accept functional macro models, for which a detailed knowledge of the constituent parts of building blocks is no longer required. The macro model characterizes the macro as a black box with functional and timing relationships between its inputs and outputs. This functional description is also referred to as a behavioral model.

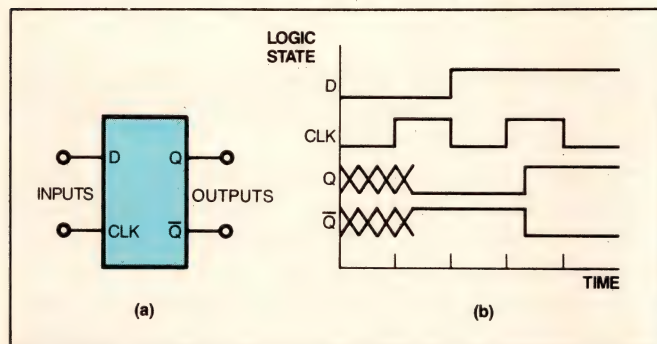


Fig 1—The waveform format for simulation vectors is familiar to most designers; it resembles the visual display of a logic analyzer. For this D flip-flop (a), the simulation vectors (b) toggle the outputs to high and low states.

You define the second input to the simulator, a description of the input stimuli that exercise the circuit, using signal states. The choice of states available to express inputs depends on the particular simulator. These states are an abstraction of the actual electrical quantities that represent logical states in the circuit. The most common set contains zero and one as logic states, X as the unknown state, and Z as the high-impedance state. Two other states, U (up transition) and D (down transition), are useful in timing simulations.

Moreover, states may have associated levels of strength, such as forcing, resistive, and high impedance. Strengths reflect the different driving capabilities of actual devices in physical circuits; for example, passive pull-up transistors on a bus structure have a resistive strength.

The simulator determines the behavior of the circuit

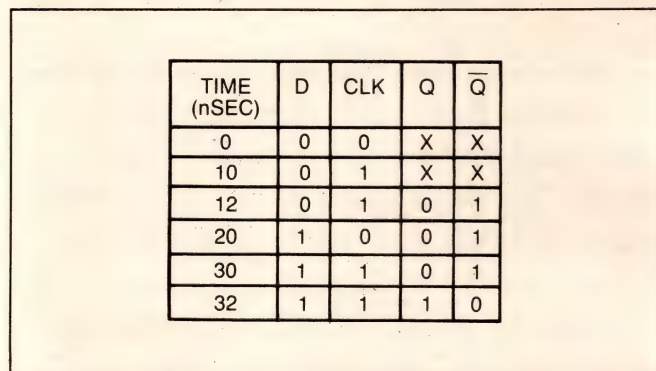
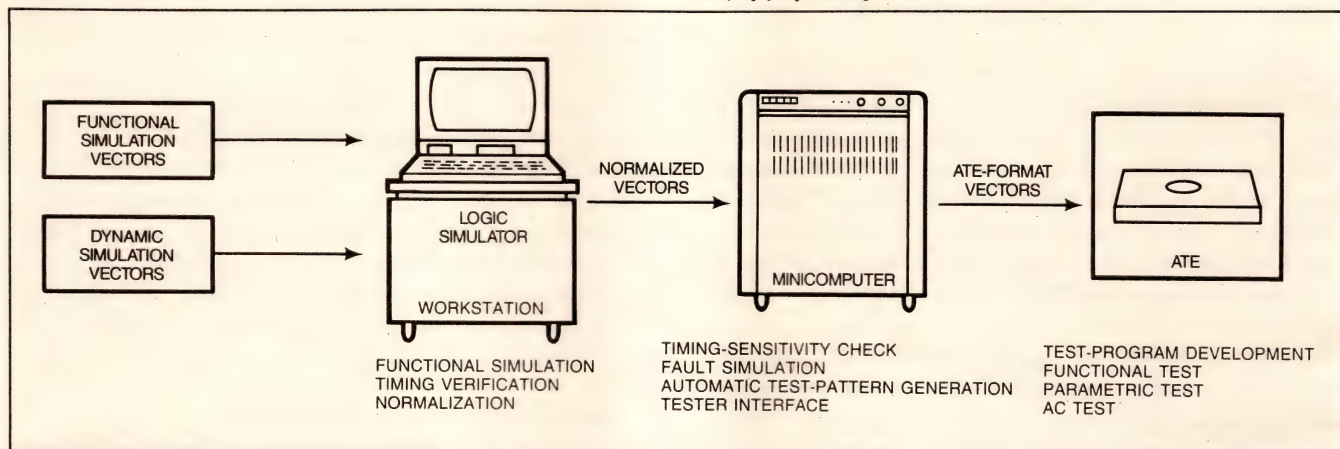


Fig 2—A tabular format for simulation vectors is more compact than the waveform representation. This table shows the vectors for the flip-flop in Fig 1.



The process of vector development begins on an engineering workstation, where you enter the functional and dynamic vector sets according to the verification needed for your logic design. You must normalize the vectors before checking timing sensitivity and simulating faults on a minicomputer or mainframe. A tester interface writes the vectors in a format compatible with ATE, and you download the vectors to the ATE for inclusion in the test program.

described in the net list by applying the input stimuli, called simulation vectors, to the inputs of macros. Based on the states and strengths of the input vectors, the macro models then assign the appropriate signals to their own outputs. In this way the simulator propagates the effect of the input vectors through the circuit to the primary outputs of the net list. Signal delays internal to the macros, as well as between the macros, can be incorporated and manipulated for worst-case simulation. You can observe any node in the circuit during the

simulation, facilitating the tracing of errors.

To write the vectors so that the simulator will understand them, you must adopt a particular format. Simulation vectors are commonly expressed in one of two formats. **Fig 1** shows a typical waveform format for a set of simulation vectors that might be used to exercise a D flip-flop. D and CLK are inputs to the flip-flop, and Q and $\bar{Q}$ are expected output values. This format resembles that of a logic analyzer and is thus easily interpreted by designers. It's good design prac-

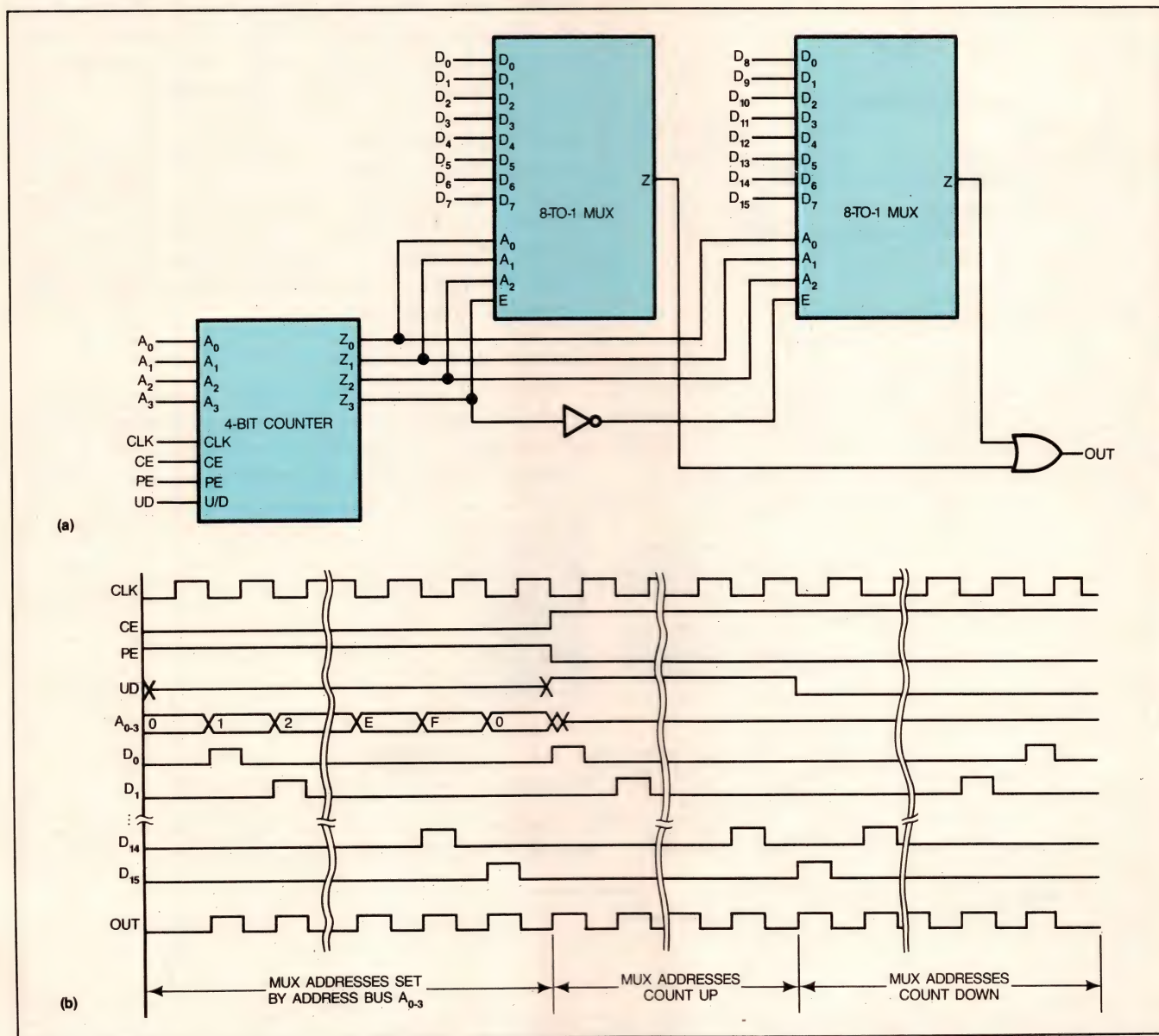


Fig 3—A circuit example (a) illustrates how a verbal description forms the basis for simulation vectors (b). The counter selects one of the data lines D₀₋₁₅ either by latching in the address at A₀₋₃ or by counting up or down.

Signal strengths allow a simulator to model the varying driving capabilities of different types of devices, such as passive pull-up transistors.

tice to develop expectation values for outputs during the vector-design process and then compare these values with simulated outputs.

The waveform format lends itself well to detailed timing development. It's not very compact, however. For a typical design, many waveforms would be required to describe a complete set of simulation vectors. A denser format is the listing of vectors in tabular form, shown in Fig 2 for the same flip-flop.

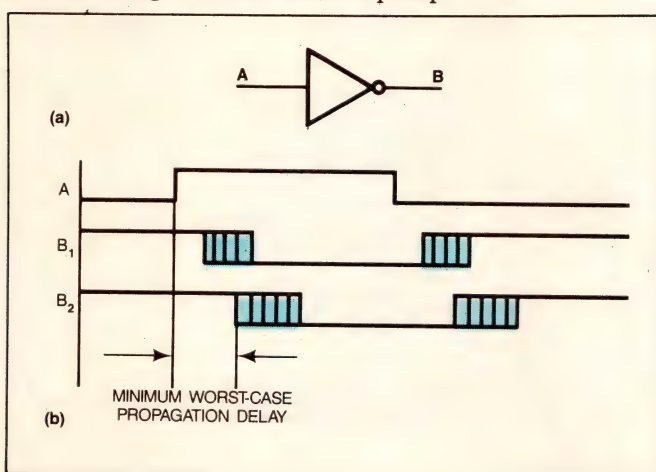


Fig 4—Circuit delays cause regions of ambiguity in the waveforms from the simulator. For an inverter (a) under typical operating conditions, circuit delays cause the transition of node B to fall anywhere within the shaded region in the waveform of B₁ (b). Worst-case operating conditions shift the ambiguity regions.

This format is called the print-on-change format: You add a line for a simulation vector only if one or more signals change. The left column of the table contains the time axis, and the columns under the signal names contain the logic states of the signal names. This tabular description is the most accurate and compact representation of signal timing in vector format, and it's available on most simulators.

One drawback to the print-on-change format is that it distorts the linearity of the time axis. Some designers instead use a periodic representation that lists vectors at a specified time interval. This form, however, is not as compact, and it loses potential timing resolution if signal changes occur between list intervals.

Depending on your simulator, other vector formats may be available: repeat statements for clocks; structures that allow synchronous vectors to change within clock cycles; and octal, hexadecimal, or decimal representations of the states of signals on buses. Regardless of the format used, the resulting description of input vectors supplies the simulator with timed input signals to apply to the net list.

Vectors check function

Once the format of the vectors is chosen, you can begin writing the vectors. The most important purpose of simulation vectors is the verification of a logic function. Take as an example of a logic function a 4-bit

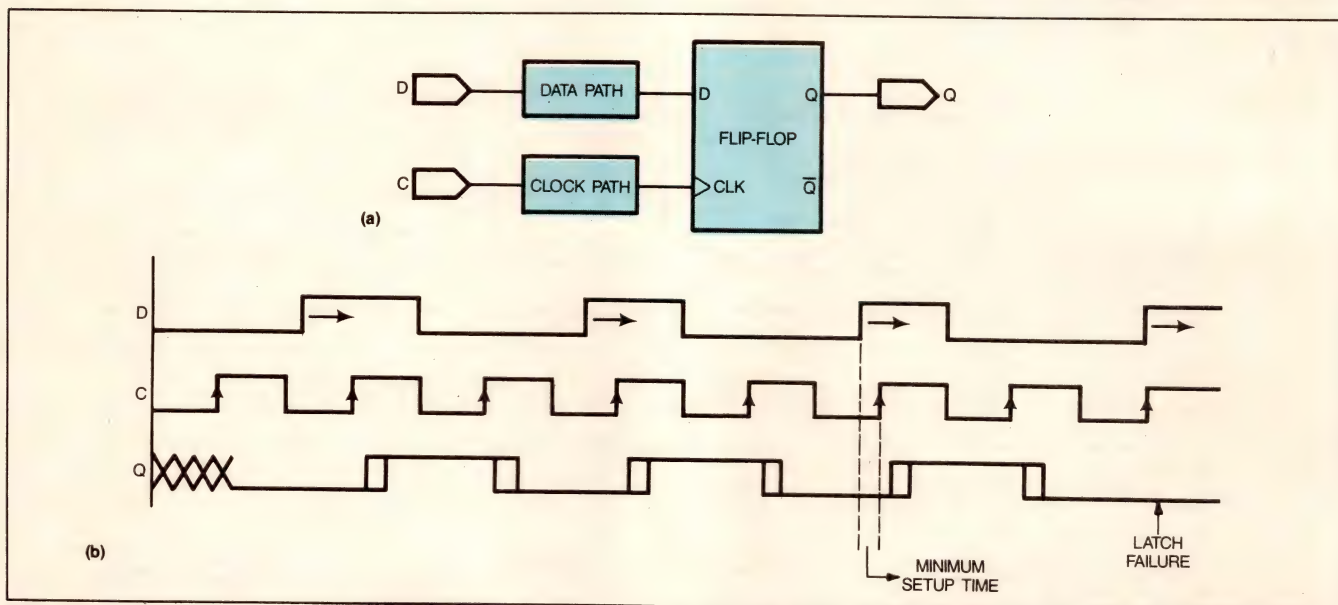


Fig 5—To determine setup timing requirements for internal storage elements, you first determine data and clock paths from primary inputs to those elements (a). Then you iteratively clock the data into the elements; each iteration reduces the amount of time between the data transition and the clock transition. The period between the edges for the last successful storage of data is the minimum setup time (b).

up/down counter that must select the data path of a 16-bit multiplexer, as depicted in Fig 3a.

A verbal description of the circuit's operation forms the basis for the simulation vectors. The outputs of the counter address one of the input data lines (D_0 to D_{15}); the inputs to the counter determine the counter's outputs. For Count Enable $CE=0$ and Parallel Enable $PE=1$, the address inputs at A_{0-3} appear at Z_{0-3} on the rising edge of the clock. When $CE=1$ and $PE=0$, each rising of the clock signal increments ($UD=1$) or decrements ($UD=0$) the value on the Z_{0-3} bus.

Fig 3b shows the associated waveforms for the functional simulation vectors. During the first 16 clock cycles, the mux addresses are set directly by the address bus, A_{0-3} . Then the counter is clocked up and down, selecting each of the addresses in order. A pulse at every addressed data channel verifies that the counter has selected the right channel. At this phase of stimulus development, the timing between inputs should be generous to simplify functional verification. Furthermore, the expected output value does not reflect the propagation delays of the circuit.

Once you're satisfied with your design and your vectors, you enter them into the simulator and start the simulation. You would find that the output in this example doesn't switch at all. You rerun the simulation to display the multiplexer outputs, which do not toggle, and then resimulate again to find that the counter outputs are correct. However, these iterative simulation steps have revealed the bug in the design: The inverter on the Z_3 line is connected to the wrong multiplexer.

This example demonstrates an important rule of thumb for debugging a logic design through simulation. Design errors tend to creep in at design interfaces and during changes in operation mode. Inside a logic array, design interfaces are located between macros that express a particular logic function. In this example, a design interface appears at the division of the 16-bit multiplexer into two 8-bit multiplexers. Consequently, functional vectors should specifically verify behavior at design interfaces. Of course, the regular function should be tested first, but then it pays to determine what happens if a counter turns over, or if the 16-bit multiplexer switches from direct addressing to counted addressing, etc.

Once you establish that your design is functionally correct, you can verify that it satisfies dynamic requirements—system speed, setup times, hold times, and propagation delays. Many logic simulators can verify

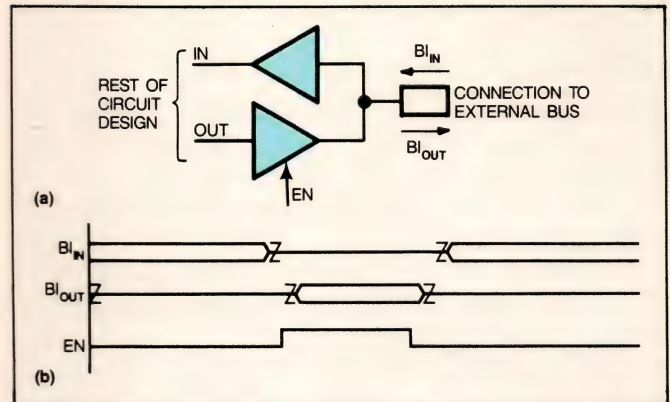


Fig 6—You can avoid bus contention by switching EN at the appropriate interval to prevent the external signal bus and the output buffer from driving the I/O node at the same time. Also include extra time margin to allow for propagation delay.

timing constraints by including delay calculations in the simulation. These simulators can flag violations of the macro's setup, hold, and pulse-width times. They can also simulate transition ambiguity, which is the window of uncertainty between the minimum and maximum delays of a signal path. These logic simulators consider the signal as unknown during the transition period.

Simulator can show delay effects

Fig 4 shows how a simulator can exhibit the effects of circuit delays in a signal path—in this case that of an inverter. For typical operating conditions, output B_1 shows minimum and maximum delay times and the window of switching ambiguity in between. Output B_2 is the same response under worst-case conditions. The difference between the two signals is a consequence of differing operating conditions.

This approach to timing verification takes advantage of the so called "on-chip tracking" effect. The underlying principle of on-chip tracking is that all propagation delays of logic paths on the same chip are affected similarly by the external operating conditions. The dominant influences are temperature and supply voltage. Typically an increase in operating temperature and a decrease in supply voltage (within the specified operating limits) increase propagation delays. Conversely, a decrease in operating temperature and an increase in supply voltage decrease propagation delays. Consequently, under worst-case operating conditions of high temperature and low supply voltage, all paths are going to be slow.

In order to cover all operating conditions, use all three selectable delay ranges: minimum, typical, and

Although waveform formats are easier for most designers to understand, tabular formats are more compact for describing simulation-vector sets.

Glossary

Bus contention—Two or more devices driving the same bus at the same time, which can result in an undefined bus state. In such a state, there is a potential for large I/O currents and considerable signal noise.

Hold time—The time required for data inputs of a clocked sequential element to be stable after a triggering clock transition.

Logic simulator—A program accepting a logic model and simulation vectors as inputs for the purpose of predicting the logic behavior of the model.

Macro—The logic building block on logic arrays. Individual macros are as complex as SSI, MSI, and sometimes LSI components.

Setup time—The time required for data inputs of a clocked sequential element to be stable before a triggering clock transition.

Simulation vectors—A set of timed input stimuli used by a logic simulator to approximate the input signals to a logic model. The simulator uses these vectors to simulate the functional and dynamic behavior of the model.

Test vectors—A set of input stimuli and expectation values that automatic test equipment uses to verify the operation of a circuit.

Timing verifier—A logic simulator that is capable of verifying a logic model's setup and hold times. It can also simulate min-max delay ambiguity.

maximum. The ranges are determined by the operating condition, and the magnitude of each range models the delay variation caused by on-chip processing fluctuations and nonuniform power distribution across the chip. If you verify your design's operation at extreme operating conditions, you gain a high level of confidence in all operating conditions between the extremes.

Generate typical and worst-case delays

You can run a timing-verification simulation for the 16-bit multiplexer described earlier to obtain the propagation delays of the data paths. This simulation can use the existing functional vectors and both typical and worst-case delay values for the design's components. The resulting output vectors show delays for both nominal or worst-case operation, and they also have

ambiguity regions associated with every transition.

Next you can determine the setup and hold times for your design's storage elements. To understand the concept of setup- and hold-time verification more clearly, consider the example shown in Fig 5. You can analyze signal paths that have setup- and hold-time requirements by reducing them to a clocked macro (eg, a flip-flop, latch, counters, etc) and a data and clock path.

Mathematically, the setup time measured at the output of the design for given operating conditions is

$$t_{\text{setup,ex}} = t_{\text{setup,ff}} + \max(t_{\text{data}}) - \min(t_{\text{clock}}),$$

and the hold time is

$$t_{\text{hold,ex}} = t_{\text{hold,ff}} + \max(t_{\text{clock}}) - \min(t_{\text{data}}),$$

where $t_{\text{setup,ex}}$ ($t_{\text{hold,ex}}$) is the setup (hold) time, seen at the chip's input pins; $t_{\text{setup,ff}}$ ($t_{\text{hold,ff}}$) is the setup (hold) time of the internal flip-flop; and t_{data} (t_{clock}) is the delay of the data (clock) path from the data-input pin to the internal data (clock) input of the flip-flop. You may need to analyze high and low transitions separately if delay data for the circuit elements is dependent on the direction of signal transitions.

You should determine setup time and hold time separately to avoid confusing the effects of each on the other. To find the setup time with the logic simulator, you run iterative simulations while reducing the time between the edge of the data input and the triggering edge of the clock. You must remember to reset the flip-flop after every attempt to set it.

The simulator initially latches the data properly and then flags a setup violation when the signal edge reaches the minimum setup time of the macro. Eventually, when the data changes state too close to the clock edge, the macro doesn't store the correct value of the data. The last successful storage of data in the macro determines the external setup time for the particular state transition of the data. You must repeat this procedure for the other transition if data propagation delays and internal setup times differ for up and down data transitions.

A similar vector sequence verifies hold times, except that the data edge now moves in on the clocking edge from the right. The last successful clocking-in of data determines the minimum hold time. To isolate and attribute the violation unambiguously when it occurs, it's good practice to write separate simulation vector sets for setup- and hold-time verification. Also, you

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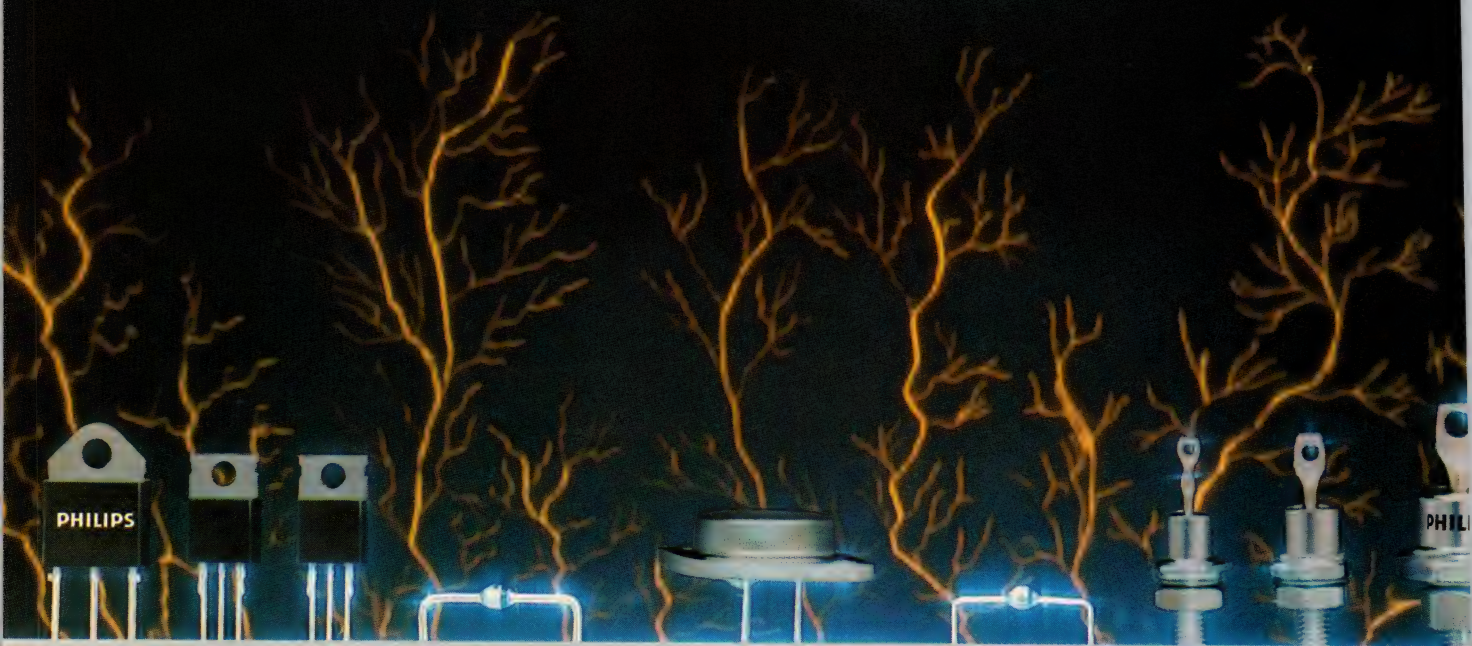
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CIRCLE NO 73

When you use the simulator for debugging, examine the behavior of your circuit at the design interfaces and operation-mode changes.

should specify ample clock periods to allow the circuit to settle between triggering edges.

In real circuits this procedure often requires many additional vectors, which establish other primary inputs to set up the data path (and sometimes the clock path). In a simulator, however, the Q output of the flip-flop can always be displayed, even if it isn't a primary output, so the measurements are easier to observe.

After you verify functional correctness and certain critical parameters like setup and hold times, you may want to simulate your logic at full system speed under worst-case operating conditions. A common dynamic simulation runs your logic at actual system speed or above while setting the macro delays to worst-case operating conditions. This simulation determines whether the part will perform in its intended application, and running your logic at frequencies higher than the intended ones establishes what margin your circuit exhibits with respect to clock frequency.

You shouldn't use vectors designed for dynamic simulation for functional testing of the physical circuit. The vectors produce failure under specific simulation conditions, so the occurrence of failure is an indicator of dynamic performance. If the vectors are used on ATE, they will most likely cause unpredictable failures because of the added constraints of the tester.

Finally, bidirectional inputs and outputs require some special attention in timing to avoid bus contention. The rule is, if the bus is armed, disarm the output, and if the output is armed, disarm the bus. For example, a bidirectional I/O buffer consists of an input buffer, which transmits any signal on the I/O pin to the interior of the array, and a 3-state output buffer (Fig 6). Also, the I/O pin typically connects to a bus signal that's external to the circuit.

Coordinate signals to avoid contention

To avoid bus contention, you must coordinate the bus-interface input signal (BI_{IN}), coming from the bus, and BI_{OUT} , from the output buffer. You switch the output buffer into high-impedance state (Z) using the output-buffer enable signal (EN), which is an input signal in most cases. Using your input vectors, you set EN to a specific value to disarm the output buffer. The buffer must generate a high-impedance signal whenever the bus is driving the pad. Similarly, when the output buffer needs to drive the I/O pad, you must ensure that the external bus signal is in the high-impedance state.

As one signal goes into a high-impedance state so the

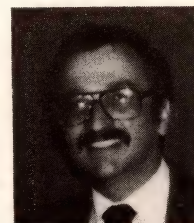
other can drive the bus, some timing margin is required. EN should become active when or after the bus is released. It should disable the output so that the high-impedance state is in effect before the bus is armed. You must include propagation delay through the output buffer and the circuitry driving the enable line. Luckily, most logic simulators will produce some warning in case of bus contention.

Once you've generated the vectors for functional and timing verification of your circuit and run your simulations, you can begin preparing these vectors for testing the physical implementation of your logic design. The second article in this series will examine the restrictions that ATE places on the development of test vectors, in particular vectors for verification of logic-array prototypes.

EDN

Author's biography

Michael Franz is in charge of advanced development at Applied Micro Circuits Corp (San Diego, CA). He performs research and development in the areas of testability, logic simulation, fault grading, and modeling. He holds a Diplom Ingenieur from the Technical University in Munich, West Germany. He also received MS and PhD degrees in engineering from the University of Wisconsin in Madison. He enjoys sailing and playing the piano in his spare time.



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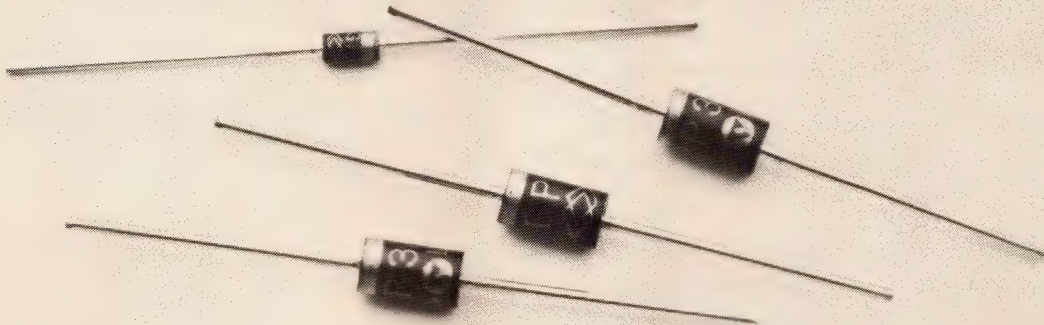
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Design a simple dual-UART-based network

With a dual UART and some simple circuitry, you can easily design an inexpensive network. Each network station has identical interface hardware and software; you can expand the network's function to cover binary-file transfer and electronic mail.

Mike Lowndes, Motorola Ltd

You can use a dual UART and some simple circuitry to design a network in which the computers on the network have continuous access to any of the peripherals. Such access is possible because the network provides local buffering at the printer-driver network nodes; this local buffering also allows for fast file transfer and effective print-spooling. The network uses a true multi-master arbitrating configuration that has identical network-interface hardware and software for every station. Furthermore, you can expand the network's function to cover binary-file transfer and electronic mail without modifying the network itself.

Designing the network

You configure the network as a bus consisting of continuous conductors that are terminated at each end of the bus. You can connect network nodes along the bus wherever you require. The MC68681 dual UART's

multidrop mode of operation (see **box**, "A look at the MC68681 dual UART") is optimized for terminal-cluster interfacing (**Fig 1**), but by adding circuitry you can develop a low-level network for ASCII-file transfer. Software enhancements can provide control data that facilitates file transfer from computers to print buffers. Further software enhancements can even provide binary-file transfer and electronic-mail functions. You can make a limited number of branches on the network to suit your installation requirements, but all the stations see exactly the same signals on the network (**Fig 2**). Each station has a unique network address that is switch selectable at the station.

The network's electrical-signal levels conform for the most part to both RS-422 and RS-232C standards, but the design includes modifications that enable half-duplex communications between any two stations on the network. The data path consists of a differentially driven twisted-pair cable. A line-terminating resistor at the end of the cable forces the data path to a logical one, a line-idle condition. A station can drive the line actively only when transmitting a logical zero. In other words, the stations are disjunctively connected (that is, connected via a wire-OR). Because it uses serial receivers/drivers (the MC3486 and 3487), the system will operate correctly even when some network stations are inoperative.

In this system, an extra differential signal pair acts as a network-free control signal; this method enables you to dispense with intermessage gaps. The scheme also allows the network's message protocol to contain significant line-idle periods during a message transmis-

Without modifying the network itself, you can expand its function to include binary-file transfer and electronic mail.

A look at the MC68681 dual UART

The Motorola MC68681 dual UART consists of two independent UART sections that are capable of operating as fast as 1M bps. The sections can operate in the multidrop mode, in which the bit in a serial character frame that would normally be a parity bit is instead designated Address/Data for logical states one and zero; thus, a disabled receiver channel in multidrop mode can accept address characters.

Typically, the CPU would compare such an address character with its own network address and, if the two matched, the CPU would enable the receiver channel for reception of data characters. By using the

multidrop mode, however, you can configure the dual UART to interrupt its host CPU when it receives such a character. You can also trigger a host interrupt by selecting from a variety of other dual-UART conditions, such as level transitions on an input pin or a counter-timer time-out. All the interrupts use the same IRQ pin, and an on-board vector register provides the host CPU with a vector number during 68000 bus-interrupt-acknowledge cycles (**Fig A**).

The MC68681's 16-bit counter-timer and the handshake protocol work together to avoid tying up your network's serial data path. The chip also offers general-purpose pins (six for input and

eight for output), some of which you can software-configure to operate as modem lines, flow-control lines, and external-clock inputs for the UART sections. Each receiver in each of these sections also provides a 3-byte FIFO buffer for incoming characters, a feature that's particularly useful in high-speed communications schemes controlled by the host CPU.

The dual UART also has an onboard crystal oscillator that, when connected to a 3.6864-MHz crystal, will provide a range of software-selectable standard rates; it will act as the chip's clock signal, which generates the DTACK signal on an asynchronous 68000 interface.

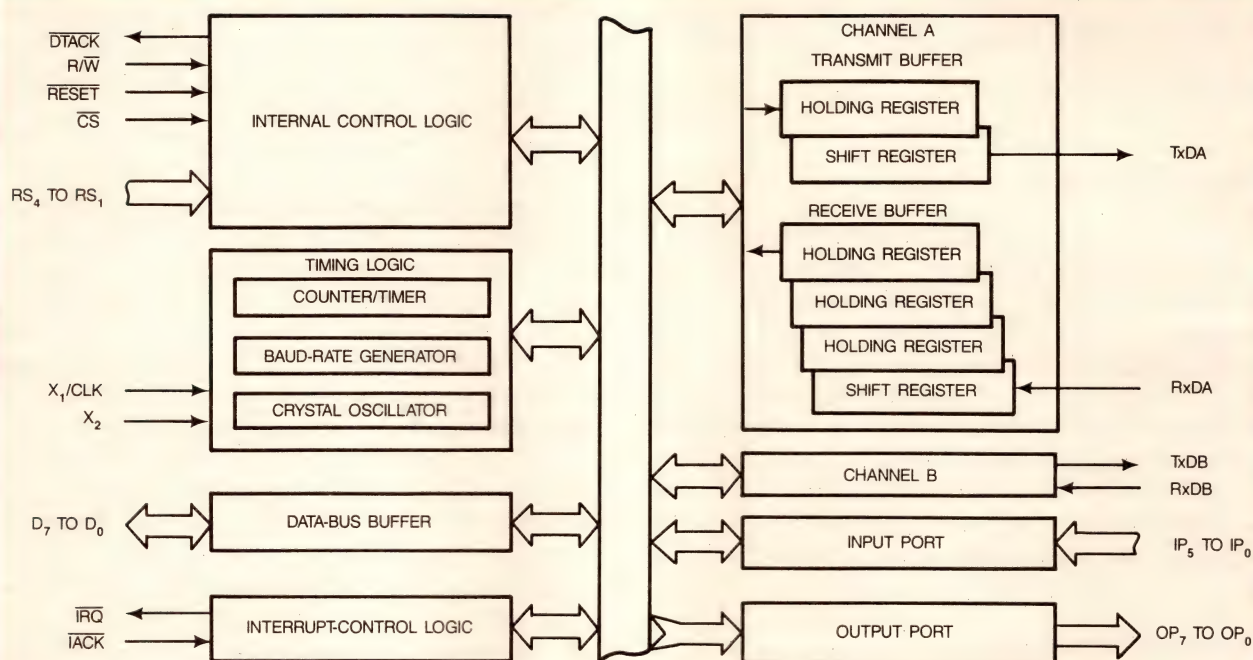


Fig A—The MC68681's independent UART sections, 3-byte FIFO buffering, and ability to operate in multidrop mode provide the basis for a number of high-speed network configurations.

sion, a useful feature if a printer driver node must spend time searching for free buffer space. The extra line drivers and receivers needed for the control signal are already available in the receiver/driver chips.

LAN uses a simple arbitration scheme

The network interface hardware illustrated in Fig 3 provides a serial interface with communication arbitration. The network-free control line (Free) at input pin IP_2 of the dual UART remains high when the network is not in use. To transmit, a station pulses its Claim line at output OP_0 of the dual UART. If the network is still free on the leading edge of this pulse, the flip-flop will set, and the Own line at input IP_0 will let the station know that it controls the network. The station can then

proceed with its transmission; when the transmission is finished, the station pulses the Release line to free the network. If the station's attempt to claim control of the bus is unsuccessful, it must try again.

This arbitration scheme is not sufficient to guarantee a station the exclusive use of the network, because propagation delays between two distant network stations mean that there is a finite temporal window during which simultaneous network claims can occur. Consequently, the first three control bytes transmitted by a station are verified by local readback at the transmitting station and by remote echo from the network destination. A mismatch or a time-out in waiting for the remote echo aborts the transmission. The content of the first three control bytes ensures that

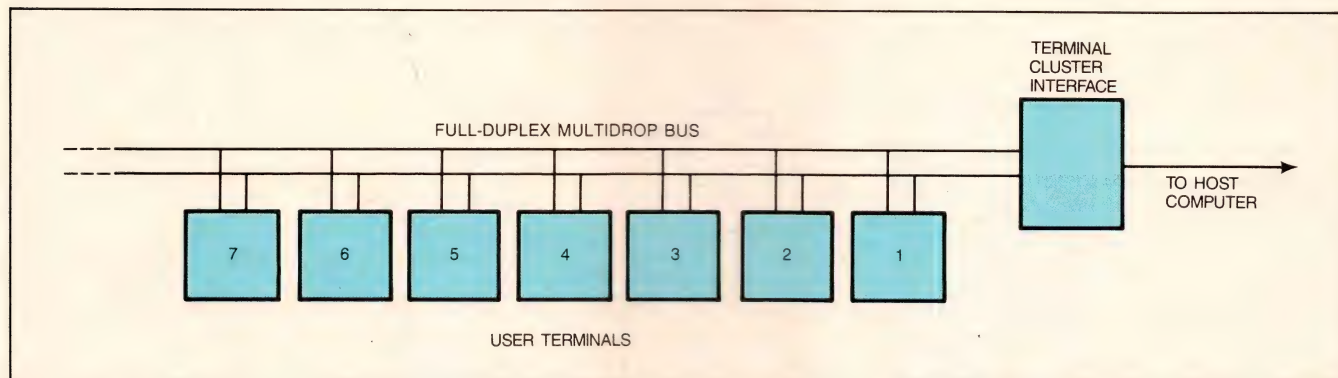


Fig 1—This terminal-cluster configuration, which uses the MC68681's multidrop mode of operation, is based on a bus that consists of continuous conductors. The conductors are terminated at each end of the bus; you can connect terminal nodes along the bus wherever you require.

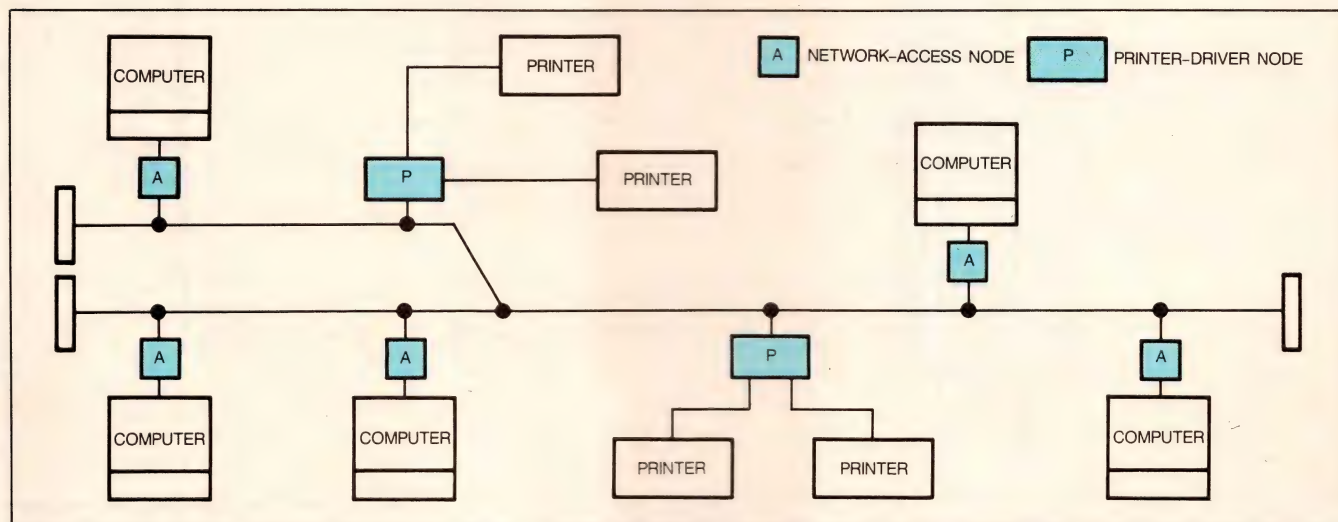


Fig 2—This dual-UART network's local-area topology allows all the stations on the network to see exactly the same signals and to have unique, switch-selectable network addresses.

You can make a limited number of branches on the network to suit your installation requirements, but all the stations see exactly the same signals.

it's virtually impossible for an undetected collision to occur; one or both of the simultaneous network claimants will back off and try again later.

Protocol also provides control

In addition to providing a means for detecting network collisions, the message protocol must also provide the control features necessary for successful transfer of data between stations. **Fig 4** illustrates the general form of a transmission packet, showing the state of the control signal, the transmitting station's data-line-drive signal, and the receiving station's data-line-drive signal. The first byte the station transmits after it successfully claims the network is the network-destination address, which is a multidrop-mode address byte that alerts the destination station.

As long as that destination station is present and active, it must echo the address within a predefined time-out period. If the echo occurs and the local and remote readbacks match the transmitted address, the transmitter sends its own address (the second transmitted byte) to the destination station, which includes the address in the transmission station's download-file copy. Note that this data and any remaining data in the transmission frame are transmitted as multidrop-mode data bytes, and are therefore ignored by everything but the destination station's dual UART. The third byte the transmitter sends is a byte count that is locally and remotely read back to specify the number of bytes in the message part of the frame.

The message data is transmitted as a continuous burst without any verification by readback, so the

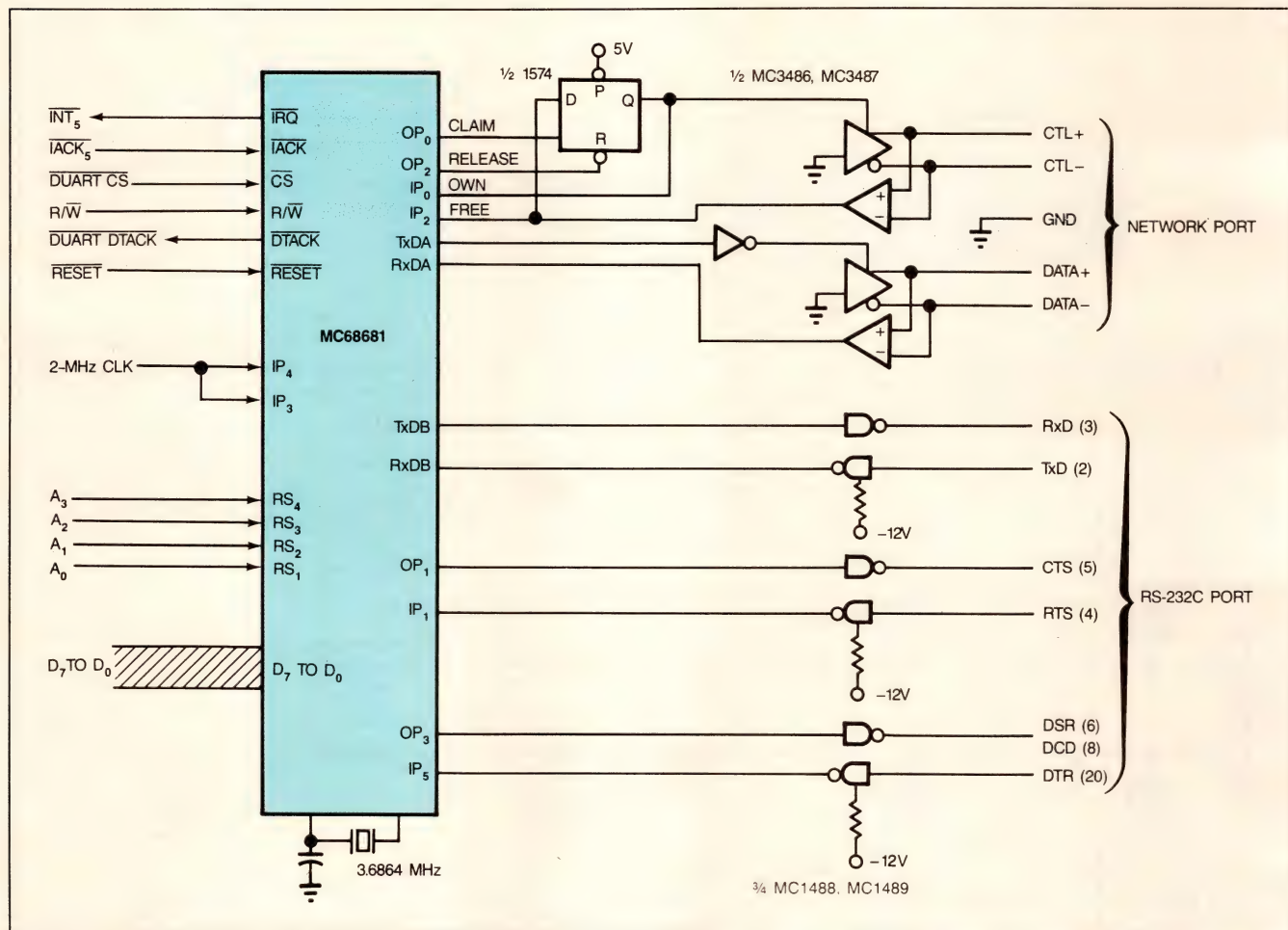


Fig 3—This network serial interface offers communication arbitration. To transmit, a station pulses its Claim line at output OP₀ of the dual UART. If the network is free on the leading edge of this pulse, the flip-flop will set, and the Own line at input IP₀ will let the station know that it controls the network.

transmission takes place at maximum network speed for most of the frame. To obtain data security and network availability, you can employ one of two schemes, both of which use a combination of message and hardware protocols. In the first scheme, the dual UART's receiver at the destination station enters a block-error mode, in which the station accumulates error bits for each character. Then, after receiving the entire message, the station checks the dual UART's status bits to determine whether any character errors have occurred.

In the second scheme, the transmitting station software-generates a block-check character (BCC) during message transmission. At the end of the message, the transmitting station sends the BCC to the destination station. Any errors in the message-data transmission create an incorrect BCC, which causes the destination station to ignore the message; the transmitting station will attempt the transmission again.

125k-bps data rate suits a small LAN

Assuming that each CPU in your network can communicate directly with its communication node's dual UART, the maximum speed at which this network can operate with a locally generated $\times 16$ serial clock is 125k bps. At 125k bps, transmission for each character—which comprises one start bit, one stop bit, one address/data bit, and eight data bits—takes 88 μ sec. Theoretically, if you were to transmit an 11,000-character print file in one burst, it would take just under 1 sec to download the file to a printer-driver node's buffer area. In practice, however, the file must be split into frames; in this case, each frame contains 125 data bytes. Because of the message-protocol and network-claiming-

mechanism overhead, the network needs about 1.2 sec to download the file.

Limiting the volume of data transferred per frame to 125 data bytes reduces system latency; that is, it enables other network nodes to use the network without having to wait for a transmitting station to transfer a whole file. Besides, if an error occurs during transmission, the originating station needs to retransmit only the part of the file that is in error.

Furthermore, these limited-volume frames ease buffer management at printer-driver nodes. Assuming that five computers are downloading 11,000-character print files at the same time, the average downloading time from each computer would be six seconds. In comparison, it takes approximately two minutes to download each file to a locally connected line printer.

Incidentally, the MC68681 can support 1M-bps operation; in such a case, you'd have to make sure that one station would always be available on the network as a serial-clock master. However, because Fig 3's network works best for a maximum of 10 simultaneous users, the 125k-bps data rate is adequate, and a serial-clock signal on the network isn't needed.

Accessing the LAN

Although a computer that could communicate directly with the dual UART could obtain a download time of 1.2 sec, most computers can't download a file that fast, because they have only 9600-baud serial ports for common external communication.

Downloading an 11,000-character print file through 9600-baud ports takes at least 14 seconds. Because other stations are on this network, the 14-sec file transfer time will increase. However, the transfer time

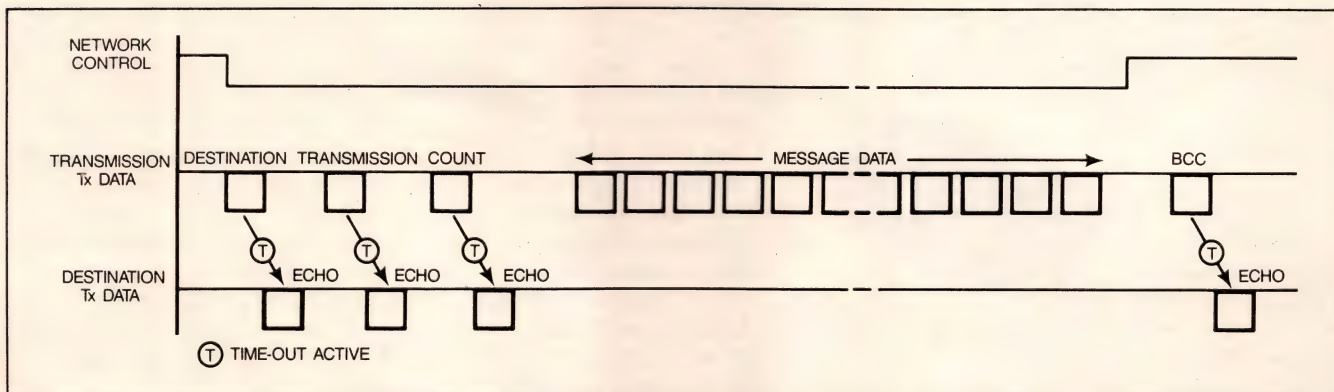
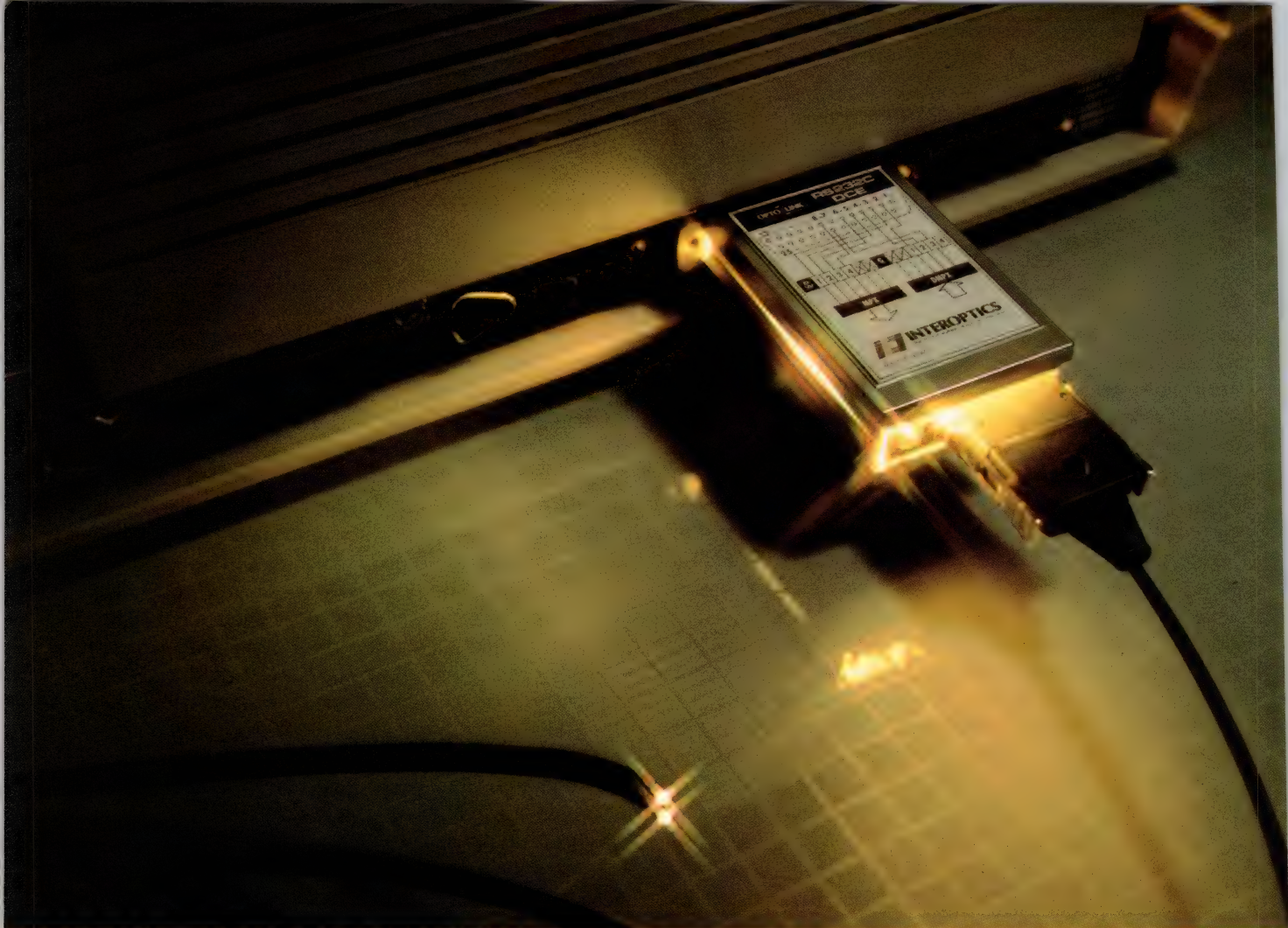


Fig 4—During the network-control pulse, the transmitting station sends out a control signal, a data-line drive signal for the destination station, and a data-line drive signal for itself. If the destination station is present and active, it echoes the source station's address byte within a predefined time-out period.



Network with Light!

In the past, computer networking could only be done using bulky coaxial cables office to office, terminal to terminal, and terminal to peripheral. And, as we all have learned, clean data was not always the rule. Power surges, radiating machine interference or any electromagnetic radiation in the vicinity was usually responsible for garbled or lost information. Lost time, frustration—we've all had to live with it . . . but that was the past.

Now, with INTEROPTICS new OPTO/LINK™ RS-232C fiber optic connector, you can network with light. Using new technology, the OPTO/LINK RS-232C, which converts data infor-

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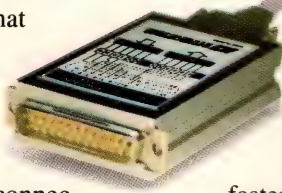
coaxial cables, with fiber optics you can design your network system without regard to outside influences. Fiber optic cables are much smaller,

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only fiber optic cables can assure you of a secure data line for sending or receiving confidential data.

This new and revolutionary, next generation transmission medium offers growth potential in Local Area Networks (LANs) that has been previously unheard of. The long term advantages are up to you and your imagination because of the full frequency spectrum available only in fiber optic technology.

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The content of the first three control bytes ensures that it's virtually impossible for an undetected collision to occur.

won't increase by more than a factor of 1.2, even when as many as five stations are performing the same downloading operation simultaneously via the 9600-baud ports. If all 10 computers were to download files simultaneously, though, each computer's download time would increase by a factor of 2, raising the file-transfer time for your 11,000-character file to 30 seconds.

After you've constructed your local-area network, you must program the dual UARTs, which appear to the programmer as sets of byte-wide registers. Some of these registers configure the operational modes, some read operating status, and others interrupt control. Generally, you must program four registers to configure a channel of the dual UART for operation in any mode; these registers select parity/error modes and character length, channel mode and stop-bit length, transmitter/receiver clock sources and rates, and channel enable/disable.

Once you set up these registers, the channel status becomes available in the channel-status register (SR). The CPU loads the transmission data into the transmit buffer (TB), and the receiver buffer (RB) accesses the first character of received data that's available in the channel's FIFO buffer. The set of registers is duplicated; the duplicate and the original are completely independent of each other, so no operation on one channel can affect the other channel.

The dual UART's counter-timer starts and stops as it reads register locations. You can preset the values in the counter-timer by writing data into its two registers, and the counter-timer can read the instantaneous value of each byte on the fly. You can also program the counter-timer clock source and mode in the auxiliary control register (ACR). In addition, you can configure the counter-timer to control the general-purpose output pin OP₂ by programming the output-port-configuration register (OPCR).

The OPCR lets you use the output pins for bit-oriented output (the default), channel flow-control signals (CTS), and clock outputs. You can configure the general-purpose input pins to act as flow-control signals (RTS inputs) and channel clock inputs or as bit-oriented inputs with associated change-of-state detectors. You can also monitor both input level and change of state, and, optionally, you can generate interrupts.

All interrupt sources in the dual UART share a common interrupt-request pin (IRQ). A vector register in the dual UART presents one vector number to the CPU during an interrupt-acknowledge cycle, when the

dual UART's IACK line is asserted. You must use an interrupt status register (ISR) to establish the source of an interrupt within the dual UART. Note that the interrupt mask register (IMR) selectively enables or disables interrupt sources without affecting the status of the ISR.

In Fig 3's network, channel A is the network port, which takes transmit and receive clocks from IP₂ and IP₄. The OP₀, OP₂, IP₀, and IP₂ UART pins provide bit I/O so that the station can claim the network. At reset, the channel A UART goes into multidrop mode, in which the UART's receiver is disabled. Channel B uses the IP₁ and OP₁ pins for automatic-flow-control signals RTS and CTS on the RS-232C serial port; IP₅ and OP₃ provide the additional control signals DSR and DTR.

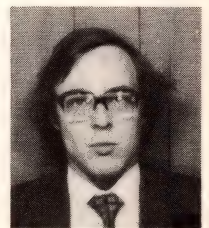
As you can see from Fig 4, the counter-timer simply acts as a timer that has an internal clock source and no output. The counter-timer's time-out status appears in the ISR; the timer doesn't act as a CPU interrupt. The initialization routine that configures the dual UART after system reset consists of 14 byte-move instructions to the dual UART's registers.

Operating the dual UART is a simple matter. The command register (CR) associated with each UART channel provides the means of enabling, disabling, and resetting receiver and transmitter sections. The CR also lets you change the channel mode, because it gives you access to both of the mode registers associated with the channel.

EDN

Author's biography

Mike Lowndes is currently employed at Insight Terminals Ltd (Wootton, Bedford, UK), where he is an engineering manager. When he wrote this article, he was a senior systems engineer for the semiconductor products sector of Motorola Ltd (Aylesbury, Buckinghamshire, UK). Mike holds a BSc in Electronics from the University of Manchester Institute of Science and Technology and is an associate member of the Institution of Electrical Engineers. His interests include church bellringing in the English style, cello playing, black-and-white photography, and drinking English beer.



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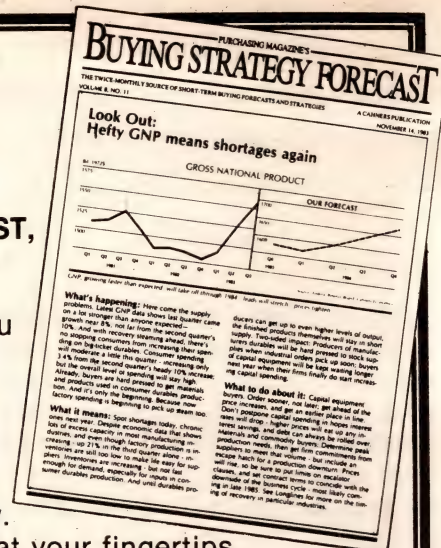
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EMR: Triple-output 22-, 42-, and 54-Watt, and quadruple-output 53- and 80-Watt, fully enclosed and shielded power supplies. High quality and low price are due in part to computer-aided design, and to use of proprietary hybrid microcircuits which greatly reduce parts population. UL recognized, CSA certified, built-in EMI filter for FCC Class B requirements.

On all models, output #1 is +5V, output #2 is +12V, and output #3 is -12V; on the two models with a fourth output, it is +24V.

ERX: World Power™ single-output 30-, 60-, and 120-Watt open frame power supplies meeting highest international safety and EMI standards. Two custom hybrid microcircuits reduce parts population, increase reliability. All sizes available with a 5V, 12V, 15V, or 24V well stabilized, adjustable output, protected by a current limiter and over-voltage protector. UL recognized, CSA certified. SELV per IEC 380 and VDE 0806. Built-in EMI filter for FCC Class B requirements.

MRM: Multi-output 40-120 Watts, flyback and forward converters in PC card (frameless) and L-chassis style, designed to meet the logic, display, serial output, and disk drive needs of CRT terminals, microcomputers and video games. All units are UL recognized and CSA certified. "KV" models are TÜV certified SELV per IEC 380 and VDE 0806. Built-in filter for FCC Class B requirements.

MP/CMP: Single-output (MP) and dual-output (CMP) 10-Watt extra compact, high efficiency switching power supplies. d-c output range of MP: 5V to 15V and 2A to 0.8A. d-c output range of CMP: output #1, +12V to +15V and 0.4A to 0.5A; output #2, -5 to -12V and 0.4A to 0.5A.

RMT/RXT/RMK/RMX/RBX: Compact, highly efficient, fully enclosed and shielded a-c to d-c or d-c to d-c switching power supplies offering stabilized outputs, overvoltage and overcurrent protection, and remote on-off. On most models, output voltages are adjustable +10% to -30%.

Series RMT (30 and 70 Watts), and RXT (150 Watts) all provide three outputs, including a basic 5V logic output which is rated at 6.0Amps in the 30 Watt models, 10 Amps in the 70 Watt models, and 20 Amps in the 150 Watt models.

Series RMK, RMX and RBX provide one output. Models are available with outputs with 2V, 5V, 9V, 12V, 15V, 24V, and 28V d-c, and a wide range of current ratings. (30Watts-600Watts) offering adjustable overvoltage and overcurrent protection and remote on-off. UL recognized; CSA certified.

RMD/RDT: Isolated, fully enclosed and shielded 30-, 50-, 70-, 125-, and 225-Watt d-c to d-c converters offering adjustable over-voltage and overcurrent protection, and remote on-off. In Series RMD, output voltages are adjustable +10% to -30%; in Series RDT, $\pm 10\%$ at all outputs. Standard inputs for Series RMD are 12V, 24V, 48V, and 110V; for Series RDT, 24V and 48V.

Series RMD provides one output and 5V, 9V, 12V, and 48V outputs are offered for all except the 110V models. For the 110V models, 15V and 24V outputs are offered.

Series RDT provides three outputs: a +5V principal output, a second output which can be either +12V or +15V, and a third which can be -12V or -15V. UL recognized, CSA certified.



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APH: High voltage (0-500V, 0-1000V, and 0-2000V) voltage/current stabilizer with automatic crossover. Separate voltmeter and ammeter. Direct front panel or remote control. Digital control of 500V and 1000V models through Kepco SN digital programmer. All models: 20 Watts.

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Kepco offers a broad choice of products for stabilizing and controlling d-c power, based on three power supply technologies.

LINEAR POWER SUPPLIES

employ a dissipative bank of power transistors or vacuum tubes, the "series pass element," which are installed between a rectified-filtered source of "raw d-c" and the output. Feedback from the output, and control signals, modify the conductance of the series pass element, stabilizing and/or modifying the output. Kepco linear power supplies, except for two series offered to the OEM, are intended for use on the laboratory bench, or in automatic test systems.

The advantages of Kepco linear supplies are:

- They offer high gain for "tight regulation" and high accuracy control, including the ability to interface with the IEEE bus.

- They function with negligible radiated or conducted EMI.

- They provide such facilities as current stabilization and operational amplifier-like control.

Their disadvantages are that they are less efficient than switching and ferroresonant power supplies with similar power ratings, and much larger and heavier than switchers.

FERRORESONANT POWER SUPPLIES'

stabilizing principle is based upon the saturation of a portion of a transformer's iron by use of a resonating capacitor, so that the output becomes a square wave-form of a constant amplitude related to the magnetic structure.

The advantages of Kepco ferroresonant power supplies are:

- They are extremely simple, rugged, and reliable, and are thus suitable for heavy duty industrial service.

- They are very efficient (65-70%).

- They offer considerable isolation from mains noise and are virtually indifferent to any outside interference.

- With respect to their power, stability, and reliability, they are quite low-priced.

Their disadvantages are that they are rather large and heavy, and their output is fixed and cannot be adjusted (except by taps).

SWITCHING POWER SUPPLIES

are based upon the conversion of an a-c input into d-c, and chopping the d-c with high frequency square pulses. The pulses are re-rectified, to produce the d-c output. Modifying the width of the pulses allows a measure of control over the voltage.

The advantages of Kepco switching power supplies are:

- They are the smallest and lightest of the three types of power supplies, because transformers operating at high frequencies can be much smaller and lighter than transformers operating at 50/60 Hz.

- They are the most efficient (65-85%).

- They can function with a wide choice of source voltages, including d-c.

- They store sufficient energy to bridge short power outages.

A basic disadvantage of most switching power supplies is that they require shielding and filtering to control EMI generated by the switching process. Most Kepco switchers have such filters built in, and the covers which are standard on some, and optionally available for most others, provide substantial shielding.

BHK: High voltage (0-500V, 0-1000V, and 0-2000V) voltage/current stabilizer with automatic crossover. User selectable slow or fast programming mode of operation. Separate voltmeter and ammeter. Direct front panel or remote control. Digital control of 500V and 1000V models through Kepco SN digital programmer. All models 200 Watts.

BOP: Bipolar operational power supplies. Operate in all four quadrants — positive or negative source, positive or negative sink — bounded by four independently adjustable, programmable limits. Full, programmable control over both voltage and current, with mode selector. Separate channels are activated for each mode. Bandwidths up to 4.5 kHz. Can be controlled either directly through front panel 10-turn bipolar controls, or remotely. Digital control through optional internal plug-in interface, or Kepco SN or TLD digital programmer*. 100-, 200-, and 400-Watt models available.

*Available fourth quarter, 1985

BOP-HV: High voltage ($\pm 500V$ and $\pm 1000V$) bipolar operational power supplies. Four quadrant operation, with independently adjustable, programmable limits. Full, programmable control over both voltage and current (from -100% to +100% of their range), with mode selector. Separate voltage and current channels. Direct front panel or remote control. Digital control through Kepco SN digital programmer. Both models 80 Watts.

CC/PCX-MAT: Plug-in, 1/6 rack width stabilizers for current (Series CC) and voltage (Series PCX-MAT). Output controlled from front panel multi-turn controls or by remote analog or digital control. Digital control through Kepco SN digital programmers. Six PCX-MAT models, outputs 7V to 100V d-c. All 14 to 20 Watts.

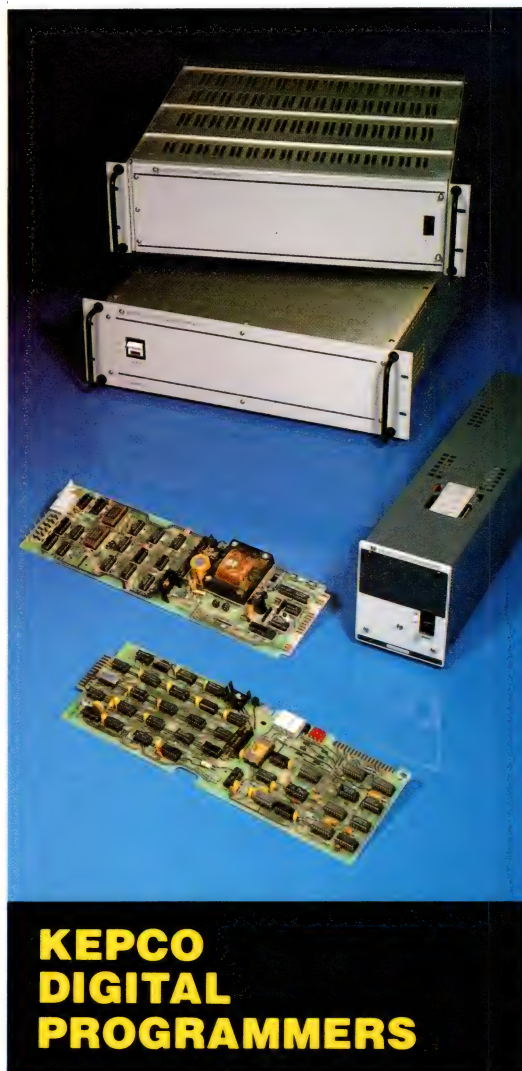
JQE: Systems-type voltage stabilizers with rectangular current limiting. Direct front-panel or remote control. Digital control of voltage through Kepco SN digital programmers. 31 models, 100, 250, 500, 1000 Watts, 0-6V to 0-150V d-c output.

MPS 620M: Triple output 70-Watt bench supply intended for the IC/ μP experimenter. Has one 0 to 6V / 0 to 5A d-c output with current limiting and overvoltage protection, continuously adjustable with a 10-turn front panel control, for digital circuits; and two tracked outputs: 0 to +20V and 0 to -20V, each rated at 0-1A, which can be used in series for 40V.

NTC: Low power (2-Watt) shunt stabilized operational inverting amplifier, intended principally as an interface between an active programming signal and a higher powered, operationally programmable power supply, to allow for control with the power supply's negative output terminal common, or grounded.

OPS IXB/OPS X: High voltage (0-500V, 0-1000V, 0-2000V, 0-3500V, and 0-5000V) voltage/current stabilizers. When used with a resistive load, they are fast-programmable. Can be controlled through their entire rated range by a 0-1mA control current, either externally generated or derived from a built-in uncommitted amplifier connected to the input summing terminal. The 500V and 1000V models can be digitally controlled through Kepco SN digital programmer.

PRR: 1000-Watt fixed output rack mounted or systems ferroresonant voltage stabilizers. Low-cost, reliable. Efficiency 70-80%. Superb line isolation. Low ripple, no spikes. Inherent current limiting and overvoltage protection. Four models: 12V/0-77A, 24V/0-42A, 28V/0-36A, 48V/0-22A d-c outputs.



Translate digital signals into analog voltage outputs that Kepco programmable power supplies understand and respond to. Output is an analog signal ± 10 Volts, which drives Kepco's programmable power supplies as scaling amplifiers. Some models (Series SN) offer 10:1 ranging. Digital input and analog output are optically isolated.

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*BOP card available fourth quarter, 1985

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MTBF values aid in predicting component failures

The concepts of reliability, failure rate, and mean time between component failures are frequently misunderstood and misused. Although related, each represents a different aspect of a component's projected operating life; together, they can help you predict how many components in a lot will fail over time.

Mark Forbes, Qualogy Inc

Although the concept of mean time between failure (MTBF) is frequently mistaken for such concepts as failure rate and reliability, MTBF is simply a statement about the *average* component in a lot; it says little, if anything, about individual components. Instead, MTBF describes what you can expect from the component lot as a whole. Unlike failure rate and reliability, and even operating life and service life (which generally connote component-replacement time), MTBF is a statistical tool, one that you can use, for example, to help compare similar products.

But besides using MTBF figures to compare products, you can use MTBF data to help predict the number of products in a lot that will fail in a given time. Such predictions are useful in making warranty estimations, ordering spare stock, or predicting the load on a factory repair depot.

Although reference books define MTBF in different ways, one common thread is, of course, that only repairable devices can have an MTBF. One of the better MTBF definitions, and the one used here, is from the *IEEE Handbook*: "MTBF is the product of the number of items and their operating time, divided by the total number of failures." The inverse of MTBF is failure rate, which is generally expressed as a percentage of a number of items per unit time (for example, 5% per year). Finally, reliability is an exponential relationship between a device's MTBF and a specifically targeted period of failure-free operation. In using these three different but related values to predict component failures, you'll find that the greater the number of repair intervals, the higher the percentage of components that fail.

MTBF and failure analysis

In applying MTBF values to manufactured devices, including solid-state electronic components, you must first consider some of the life-cycle characteristics of these devices. The manufacturing process yields a large percentage of failures caused by component weaknesses that show up in the first few hours of operation. These failures (infant mortalities) result from the stress applied to a device during its initial operation—the burn-in period. Once you eliminate the weak devices, those that remain exhibit the long-life characteristics that you expect from solid-state devices.

However, once solid-state components begin to wear out, the failure rate increases dramatically (**Fig 1**). When using an MTBF value, you must recognize that the value applies to the constant failure rate during the

MTBF is a statement about the average component in a lot; it says little about individual components.

normal life of the component. Accordingly, MTBF is a statistical tool that applies only to the time between the end of burn-in and the beginning of wear-out.

One common misconception about MTBF is that a given device should operate for roughly one MTBF period before failing. As Fig 2 shows, however, 63.2% of the units produced will experience at least one failure

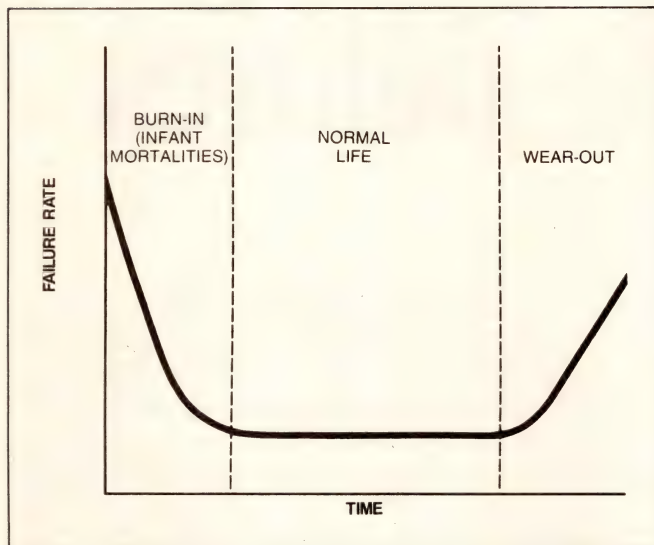


Fig 1—For the average solid-state electronic component, the highest mortality rates occur during the burn-in and wear-out periods. MTBF is a statistical tool that describes typical component behavior during the normal-life period.

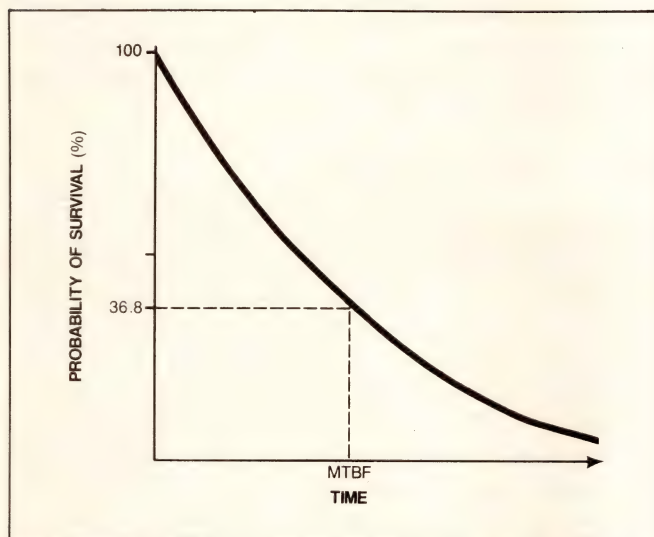


Fig 2—The probability of component survival over time is an exponential distribution. The probability that a component will survive one MTBF period is 36.8%; the probability of failure is 63.2%.

in one MTBF period; thus, only 36.8% will operate through the entire MTBF period without failure. More important, of the 63.2% that fail, some will fail more than once. Furthermore, when enough devices are produced, some will fail almost immediately regardless of the length of the MTBF. Referring to Fig 2, you can estimate that a device with an MTBF of 30 years, if produced in large quantities, yields about 0.3% failures in the first month of operation. However, this curve also indicates that about 3.6% of the units will operate for the next 100 years.

Reliability and probability of survival

Besides failure rate, MTBF is sometimes confused with reliability. Reliability (R) is an exponential relationship between a device's MTBF and a specifically targeted period of failure-free operation: R is the chance that a device will survive to the specified target date. For example, when R is 0.95 for a 5-year period, either a given device has a 95% chance of operating for five years without failure, or 95% of such devices will operate for at least five years without failure. Both interpretations are valid.

In the reliability relationship $R = e^{-(t/m)}$, t is the target period of time and m is MTBF. To avoid misinterpretation of MTBF values, consider the following comments:

- MTBF is the mean time between successive failures of a component. The term "successive failures" implies that you can repair the unit.
- MTBF is different from operating life, service life, or other indices that generally connote re-

TABLE 1—REPAIRS VS FAILURES

REPAIR INTERVALS	TOTAL FAILURES
1	0.63212
2	0.7924698
3	0.834367
4	0.8535459
5	0.8645299
6	0.8716436
7	0.8766254
8	0.8803084
9	0.8831418
10	0.8853889
50	0.9010728
100	0.9029732
250	0.9041076
500	0.9044856
1000	0.9046728
5000	0.9048276

placement time. Operating life, for example, is the more pertinent measure for a component that operates continuously.

- When the failure rate is constant, the probability of a component operating without failure for a time equal to or greater than the MTBF is only 36.8%; not 50%, as many designers believe.

Furthermore, an increase in MTBF doesn't yield a proportional increase in reliability. The probability of component survival increases slowly as MTBF grows. For example, if t equals one year, the MTBFs (in years) required for various R values are as follows:

MTBF	R
5	0.82
10	0.90
20	0.95
100	0.99

Thus, to increase the reliability factor by four percentage points, you must increase MTBF by a factor of 5, from 20 to 100 years. In comparison, doubling the MTBF from five to 10 years yields an 8-percentage-point increase in reliability. Although many designers use MTBF in making reliability decisions, R itself—the probability of survival for a specified time—is actually a more appropriate index for such decisions.

Although R indicates that 63.2% of the components produced at a given time will fail in one MTBF period, some of the units included in the 63.2% figure will fail more than once. To simply use 63.2% as a prediction for component failure results in a significant underestimation. Note the distinction—63.2% of the units produced will fail, but you can expect a higher percentage of failures as you repair the failed units. The calculations to determine this higher probability of failure are based on the premises that all failures are repairable and that the distribution of failures remains exponential: ie, $R = e^{-(t/m)}$.

As defined by the exponential distribution, the probability of surviving one MTBF period is $R = e^{-1}$, or 36.8%. Again, Fig 2 illustrates this distribution, and 63.2% is the probability of failure. However, once a part is repaired and placed back in service, a new MTBF period begins. During the new MTBF period, failures will occur, and some of these failures will occur before the first MTBF period expires; in other words, some parts will fail more than once during the original MTBF period.

For example, assume that you purchase a large

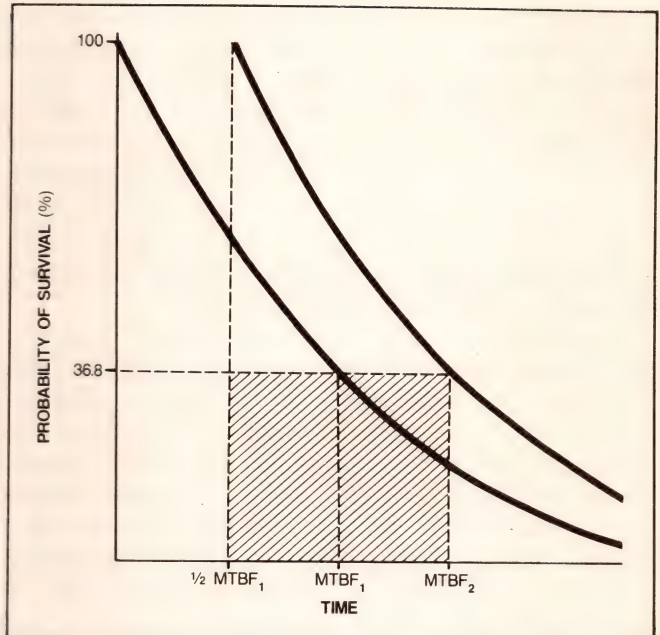


Fig 3—When you repair failed components at a period that is one-half the duration of $MTBF_1$ and then place those components back into service, a new MTBF period begins. During the new period (shaded area), which lasts until $MTBF_2$, failures will occur; some of these failures will occur before the $MTBF_1$ period expires.

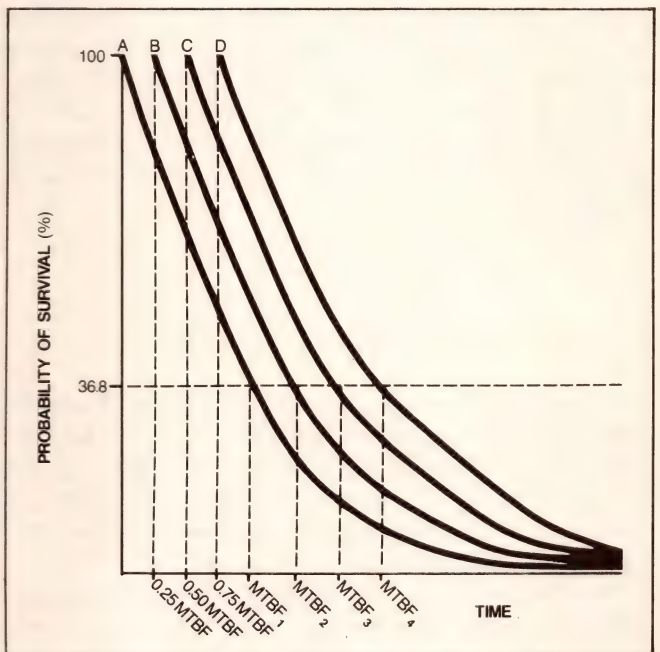


Fig 4—By decreasing the intervals between component-repair periods, you increase the total probability of failure (P_f). Assuming four equally spaced repair intervals, the P_f by MTBF is 63.2%+11.7%+6.8%+3.0%, or 84.7% of the number of units produced.

One common misconception about MTBF is that a device should operate for roughly one MTBF period before failing.

number of devices produced at $t=0$. Now, assume that as the devices fail, you place them in a warehouse and repair all the failures halfway through the MTBF period. In Fig 3, the vertical dashed line at $\frac{1}{2}$ MTBF shows the reintroduction of these units and their new MTBF curve. Of course, when the original reliability curve reaches the $MTBF_1$ value, the repaired components are only halfway to the $MTBF_2$ mark. Again, these repaired units will exhibit the same failure characteristics as did all the units from $t=0$.

The percentage of products that fail is represented by the probability of failure, P_f . When $t = \frac{1}{2}$ MTBF, then P_f equals $1 - e^{-0.5}$, or 0.393. So the second reliability curve begins with the population of 39.3% of the original component population. Of this 39.3%, another 39.3% will fail by $MTBF_1$, a point occurring halfway through the period ending at $MTBF_2$. (This period is represented by the shaded area in Fig 3.) Accordingly, this new percentage of failures is 0.393×0.393 , or 15.4%. Therefore, for only one repair instance, the total percentage of failures is $0.632 + 0.154$, or 78.6%—a figure significantly greater than the 63.2% failure probability for components that aren't repaired and reused during the original MTBF period.

Furthermore, the probability of failure continues to rise as the number of repair intervals increases. Fig 4 shows the component-reliability curves for repairs made four times during an MTBF period. (The curve beginning at $t=0$ of $MTBF_1$ is labeled curve A; curves beginning at the subsequent time intervals are labeled B, C, and D.) The failure analysis from $t=0$ is as follows:

$$t/m=0.25: 1 - e^{-0.25} = 0.221$$

$$t/m=0.50: 1 - e^{-0.50} = 0.393$$

$$t/m=0.75: 1 - e^{-0.75} = 0.528$$

$$t/m=1.00: 1 - e^{-1.00} = 0.632$$

When 22.1% of the units fail by $t/m=0.25$ and are then repaired, by $t/m=1$ ($MTBF_1$ on curve A) these units will be three-fourths ($t/m=0.75$) of the way into the $MTBF_2$ (curve B) period. The number of failures in the curve-B repaired group of components by the end of $MTBF_1$ will be $0.221 \times (1 - e^{-0.75})$, or 11.7%.

For those components repaired halfway through the $MTBF_1$ period, the number of failures is the total failures from $t=0$ to $MTBF_3$, less the failures just accounted for in the first quarter: $0.393 - 0.221 = 0.172$. Of this 17.2%, the number of repaired units that will fail by $MTBF_1$ is $0.172 \times (1 - e^{-0.5})$, or 6.8%. Accordingly, the number of failures by $MTBF_4$ is

$0.528 - 0.393 = 0.135$. And the number of these repaired units to fail by $MTBF_1$ is $0.172 \times (1 - e^{-0.25})$, or 3.0%.

Probability of failure rises

Thus, the total probability of failure, including the multiple failures and assuming four equally spaced repair intervals, is $63.2\% + 11.7\% + 6.8\% + 3.0\%$, or 84.7%. Note that the 84.7% figure refers to the original number of units on hand at $t=0$, not to the number of the units produced and repaired.

The general form of the equation for p equally spaced repair intervals is:

$$P_f = (1 - e^{-1}) +$$

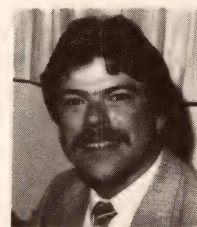
$$\sum_{n=1}^p \left[\left(1 - e^{-\frac{n}{p}} \right) - \left(1 - e^{-\left(\frac{n-1}{p} \right)} \right) \right] \left(1 - e^{-\left(1 - \frac{n}{p} \right)} \right), \quad (1)$$

where n is the fraction t/m , and p is the number of repair intervals, including the one at $MTBF_1$. So, for the Fig 3 example, p equals 2; for the Fig 4 example, p equals 4, and so on.

To determine the convergence of Eq 1, calculate the limit as p approaches infinity. This limit was approximated with a program written in Basic, the results of which are shown in Table 1. For a realistic number of repair intervals, the equation converges to roughly 0.9, or 90%, and not to 63.2% (as indicated by the probability of failure with no repair intervals). **EDN**

Author's biography

Mark Forbes is a product manager at Qualogy Inc in San Jose, CA, where he is involved in product marketing and the development of application notes. Mark obtained his BSEE degree from Bradley University and holds one patent. He enjoys skiing, photography, amateur radio, and sports officiating.



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674	335688 NOP (S)
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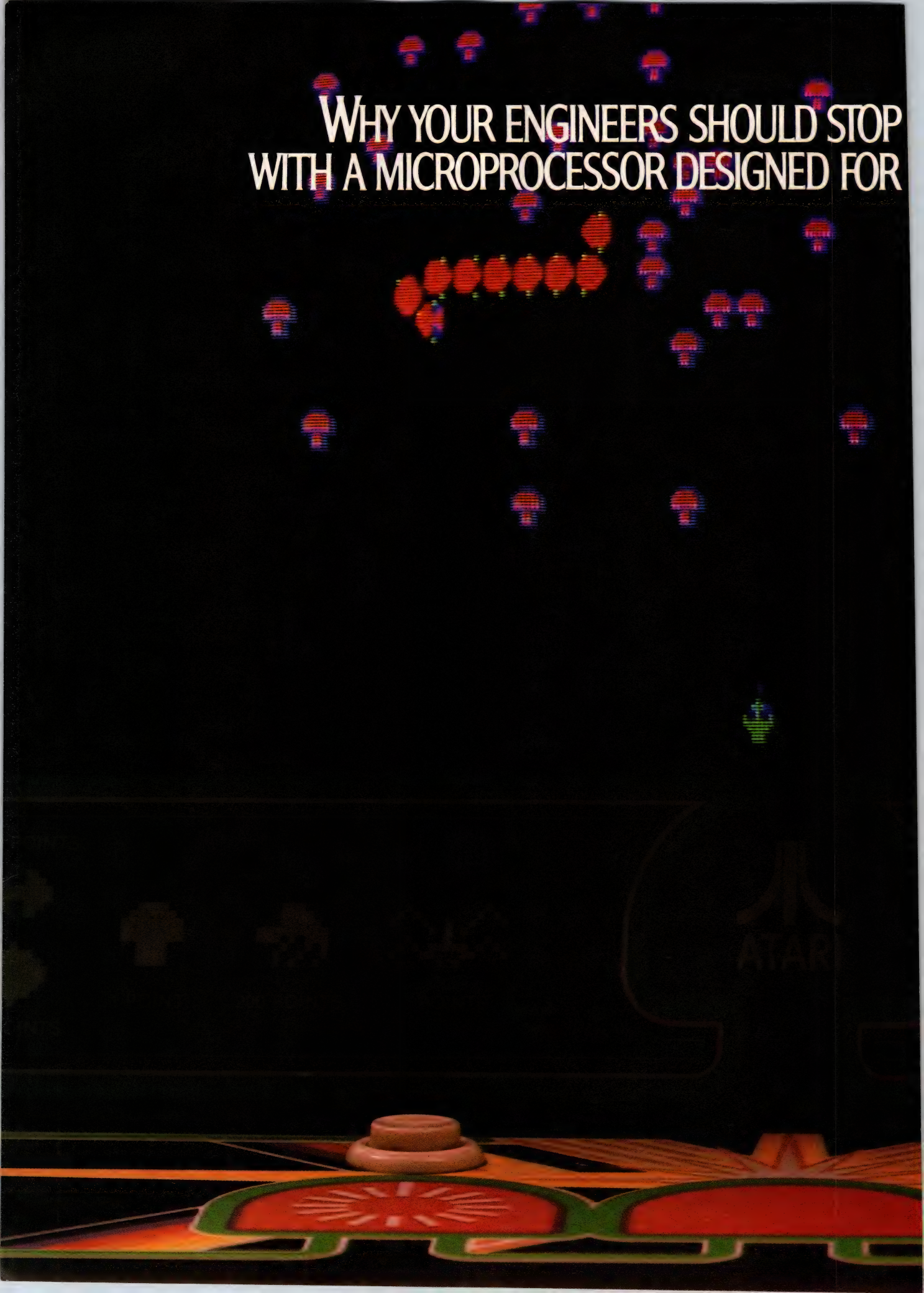
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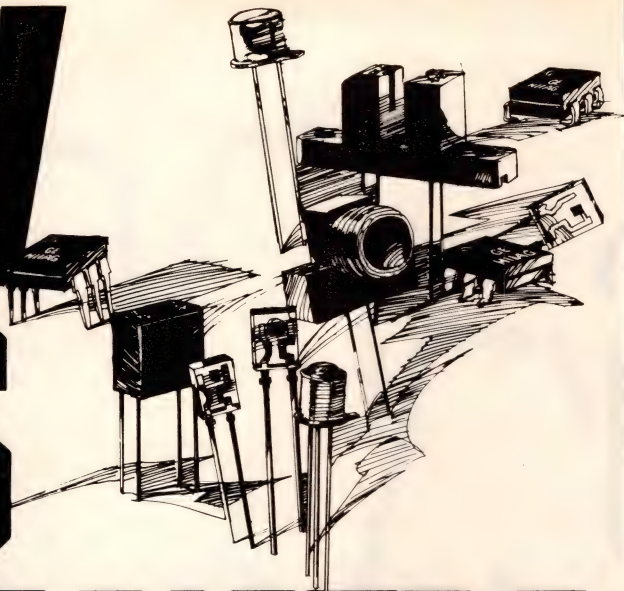
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Understand probe resistance to ensure accurate measurements

When you choose a probe for an oscilloscope measurement, consider the effects of the probe's resistance on your circuit. By selecting the right probe for your circuit, you can avoid measurement errors.

William Escovitz, *Hewlett-Packard Co*

When you use a scope probe to test a circuit, the probe becomes part of that circuit and affects its performance. Thus, you must be sure to choose the proper probe for a particular oscilloscope measurement. Otherwise, the scope probe could have a profound influence on the measurement results. For example, if you attempt to measure a high-resistance circuit node with a scope probe of insufficient resistance, any or all of the following problems may occur:

- The dc values at some circuit nodes may change significantly, even though the circuit under observation still works.
- Significant changes may occur in the output waveform.
- The circuit may not work.

To see how probe loading can cause such effects on a circuit, consider the wideband amplifier in **Fig 1**. The circuit includes an op amp and a high-frequency hybrid.

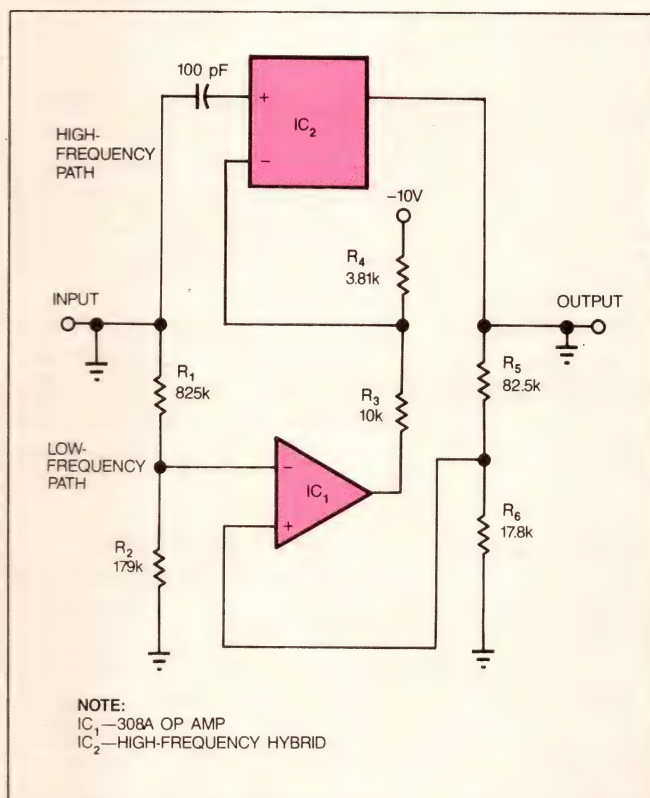


Fig 1—You can see the effects of probe loading by probing different nodes in the wideband amplifier contained in the input pod of an HP 54003A scope probe. The circuit has nodes whose impedance can be as high as 150 k Ω . If you take measurements with probes of insufficient resistance, you might change the characteristics of the circuit.

A probe's resistance can load your circuit to the point where it will not operate.

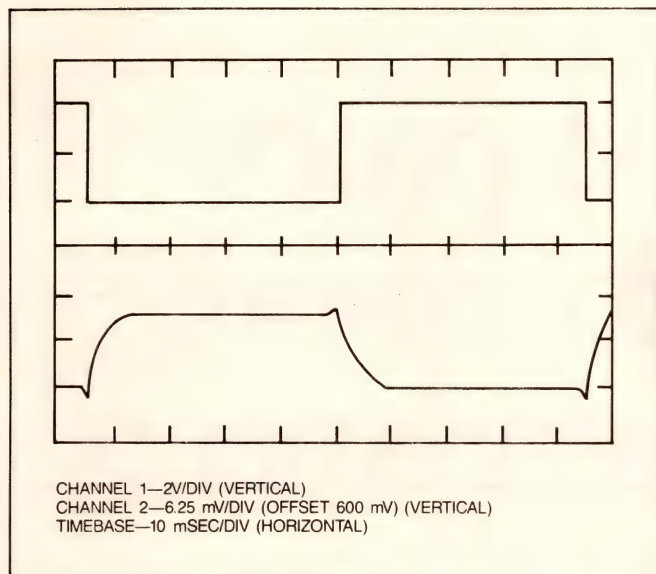


Fig 2—When you apply an 11-Hz square wave to the amplifier in Fig 1, you get the traces shown here. The top trace is the amplifier output. The bottom trace is at the low-frequency input of IC₂ (the junction of R₃ and R₄). Correct output waveforms do not guarantee that the circuit is operating properly.

The amplifier's dual-path circuit passes high-frequency signals (>20 Hz) through the capacitor and the unity-gain high-frequency hybrid, IC₂. Low-frequency signals (<1 MHz) pass through the op amp (IC₁) and then through the low-frequency input of IC₂. The roll-off frequencies of the two signal paths overlap, making overall frequency response uniform.

The junctions of the three resistor pairs (R₁ and R₂, R₃ and R₄, and R₅ and R₆) are high-impedance nodes, which are sensitive to the resistive load of an oscilloscope probe. When you test op-amp circuits that have similar nodes, you should choose a high-impedance probe to test the circuit.

Low probe resistance shifts internal voltages

The following examples of probes and the effects of their resistance on the test circuit in Fig 1 demonstrate the relationship between probe resistance and oscilloscope measurements. The 10-k Ω probe in the examples is an HP 54001A, 2-pF probe with a 1-GHz bandwidth; the 1-M Ω probe is an HP 54003A, 8-pF probe with a 300-MHz bandwidth (this probe is an accessory to the HP 54100A/D digitizing oscilloscope); and the 10-M Ω probe is an HP 10014A, 10-pF probe with a 300-MHz bandwidth.

When you use the 1-M Ω probe to monitor the junction of R₃ and R₄ (a node with a 3-k Ω impedance), the

normal dc output of IC₁ is 0V and the low-frequency input of IC₂ is -7.5V. As you would expect, channel 2's waveform is a bandwidth-limited square wave (Fig 2).

If you use the 10-k Ω probe to take the same measurement, the output waveform is still correct. However, the dc output of the operational amplifier is -7.5V instead of 0V; -7.5V is close to the minimum voltage

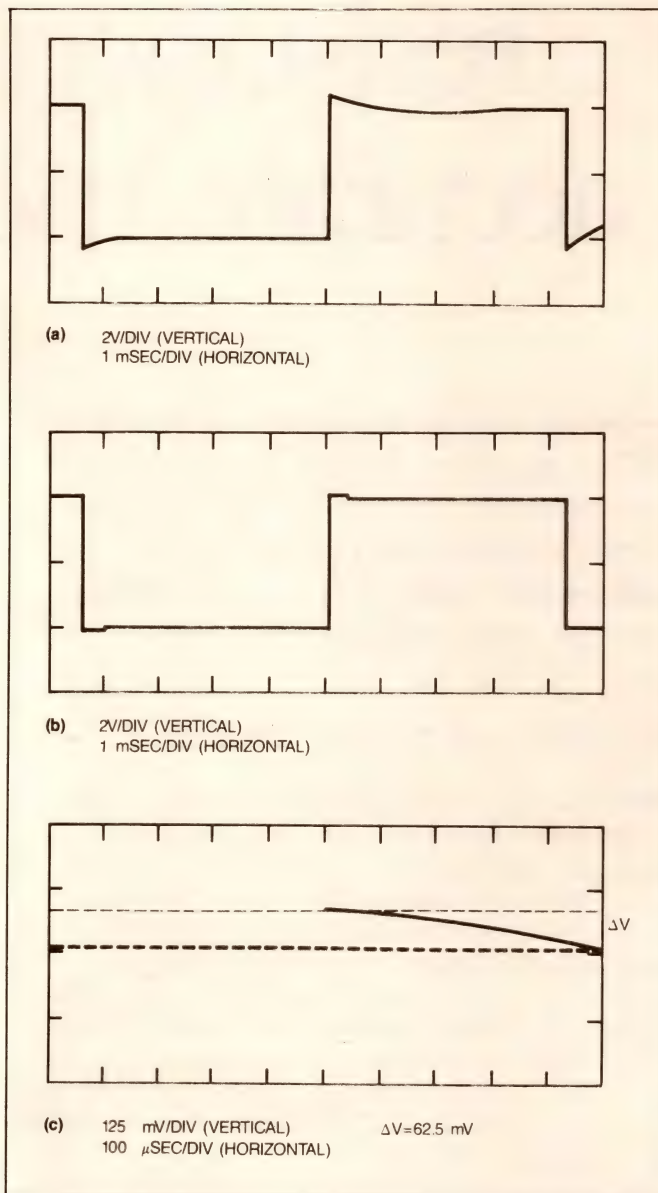


Fig 3—Resistive loading of the 1-M Ω probe causes a gain mismatch between IC₁ and IC₂ that results in the droop (a). Taking the same measurement with a 10-M Ω probe reduces the error caused by the probe to 1.5% (b). Expanding the scale quantitatively shows the reduction in the measurement error. The droop (ΔV) is 62.5 mV, or approximately 1.5% of the 4V p-p value of the waveform (c).

IC₁ can provide and far from the design voltage of 0V dc. Thus, using a probe whose resistance is too low significantly upsets the circuit's internal voltages, even though the circuit still works.

You might be tempted to conclude that the measured -7.5V is the valid operating level and that your design voltage of 0V was a design error or a circuit malfunction. In this case, however, the probe caused the shift in the dc levels. So, if your measured values vary greatly from your design values, be sure to check your probe's impedance.

Insufficient probe impedance shifts gain

Besides changing the dc levels, probe loading can make circuits inoperative. In Fig 1, the node impedance of IC₁'s noninverting input is approximately 15 kΩ. If you use the 10-kΩ probe to take a measurement at the noninverting input, you will double the low-frequency gain of the circuit. Attaching the probe from IC₁'s noninverting input to ground reduces R₆ from 17.8 to 6.4 kΩ. When you insert the reduced value of R₆ into the equation

$$\frac{R_2(R_5 + R_6)}{(R_1 + R_2)R_6} = 1, \quad (1)$$

you see that the circuit's low-frequency gain increases from 1 to 2.5. The circuit cannot operate with that much gain, so it latches up.

Reduce errors by changing probes

You can reduce measurement errors by using a probe that has higher impedance. In the test circuit in Fig 1, the impedance of the inverting input of the op amp is approximately 150 kΩ. If you probe the inverting input with the 1-MΩ probe you can see that the circuit's output is changed (Fig 3a), because the shunt resistance of the probe has reduced the low-frequency gain. When you use the 1-MΩ probe to look at the inverting input, the probe's 1-MΩ resistance reduces R₂'s value to 152 kΩ. Insert R₂'s new value in Eq 1; you'll see that the low-frequency gain is now 0.87. The low-frequency gain of 0.87 and the high-frequency gain of 1 causes the drooping response that you see in Fig 3a.

If you reduce probe loading at the inverting input by using a 10-MΩ probe to take the measurement, the gain mismatch caused by the probe will be 1.5%, which will show up in Fig 3b as a slight break in the square wave.

Using the high-resistance 10-MΩ probe essentially eliminates the effects of probe loading at the inverting input.

By magnifying the waveform, you can measure the reduction in the measurement error quantitatively. Fig 3c shows the circuit's output magnified from 2 V/div to 125 mV/div (the sweep speed has been increased to 100 μsec/div). Two voltage markers, one at the peak value and one at the long-term value of the square wave, measure the wave's droop. The change in voltage indicated by ΔV is 62.5 mV, or approximately 1.5% of the waveform's 4V p-p value.

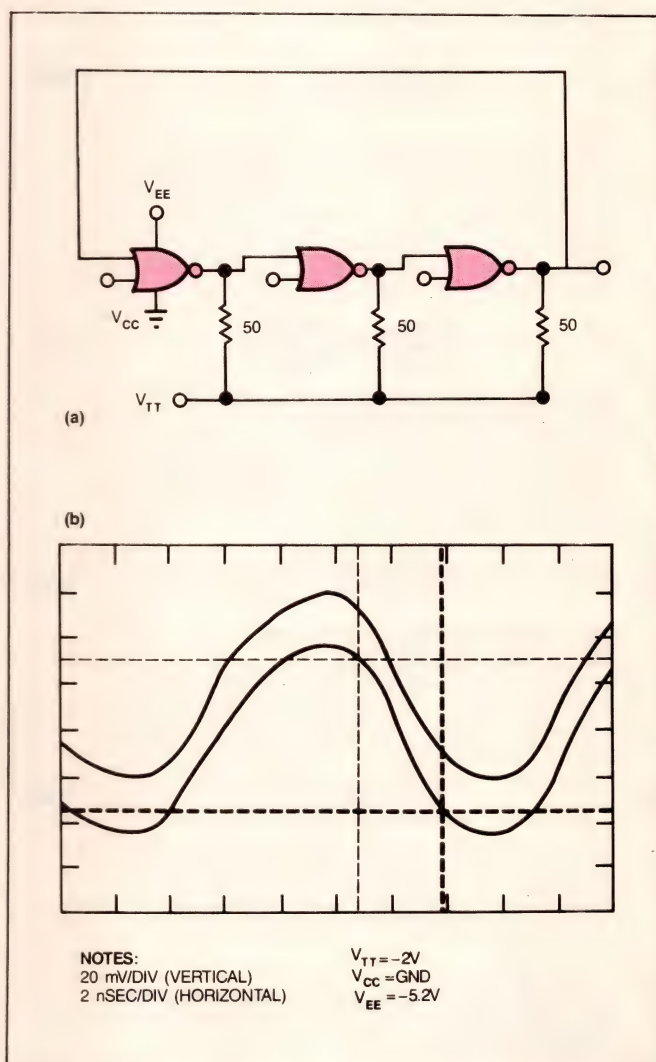


Fig 4—An ECL NOR-gate ring oscillator (a) is a high-frequency circuit that is relatively insensitive to a probe's tip capacitance. The scope traces (b) show that you can probe this ECL circuit with a 500Ω, 0.7-pF probe (top trace) or a 1-MΩ, 8-pF probe (bottom trace). The markers show a 90 to 10% fall time of 3.15 nsec.

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You can use a high-resistance probe to take measurements of circuits that have frequencies as high as 300 MHz, as long as the probe's tip capacitance doesn't load the source impedance. When you use the 1-M Ω probe, for example, make sure that the source resistance is <70 Ω at 300 MHz.

To examine the effects of probe capacitance on high-speed circuits, consider the ring oscillator in Fig 4a. The circuit includes three 10K ECL NOR gates. ECL outputs have very low impedance and are relatively insensitive to the 1-M Ω probe's 8-pF load capacitance.

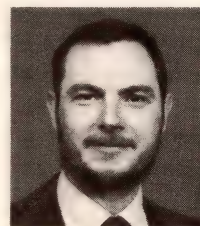
When you probe the oscillator circuit with the 1-M Ω probe and a 500 Ω , 10 $\times$ resistive-divider probe, you get the waveforms shown in Fig 4b. The output waveforms of the two probes are essentially the same.

Manufacturer's specifications for 20 to 80% rise and fall times for 10K ECL devices are typically on the order of 2 nsec. The traces in Fig 4b show that the rise and fall times for the probes are 2.2 and 2.04 nsec, respectively. When 0.7- and 8-pF probes were used in the oscillator circuit, the oscillator period was 12.93 and 12.99 nsec, respectively. Although the 1-M Ω , 8-pF probe is intended for low current loading at low frequencies, when it was used to probe a high-speed ECL circuit, it produced the same timing measurements as the 0.7-pF probe did.

Finally, remember that you can usually represent a scope probe as a resistor in parallel with a capacitor. Redrawing the schematic of your circuit with the probe's resistance and capacitance added, and analyzing the circuit's behavior, will help you choose the proper probe for measuring your circuit. **EDN**

Author's biography

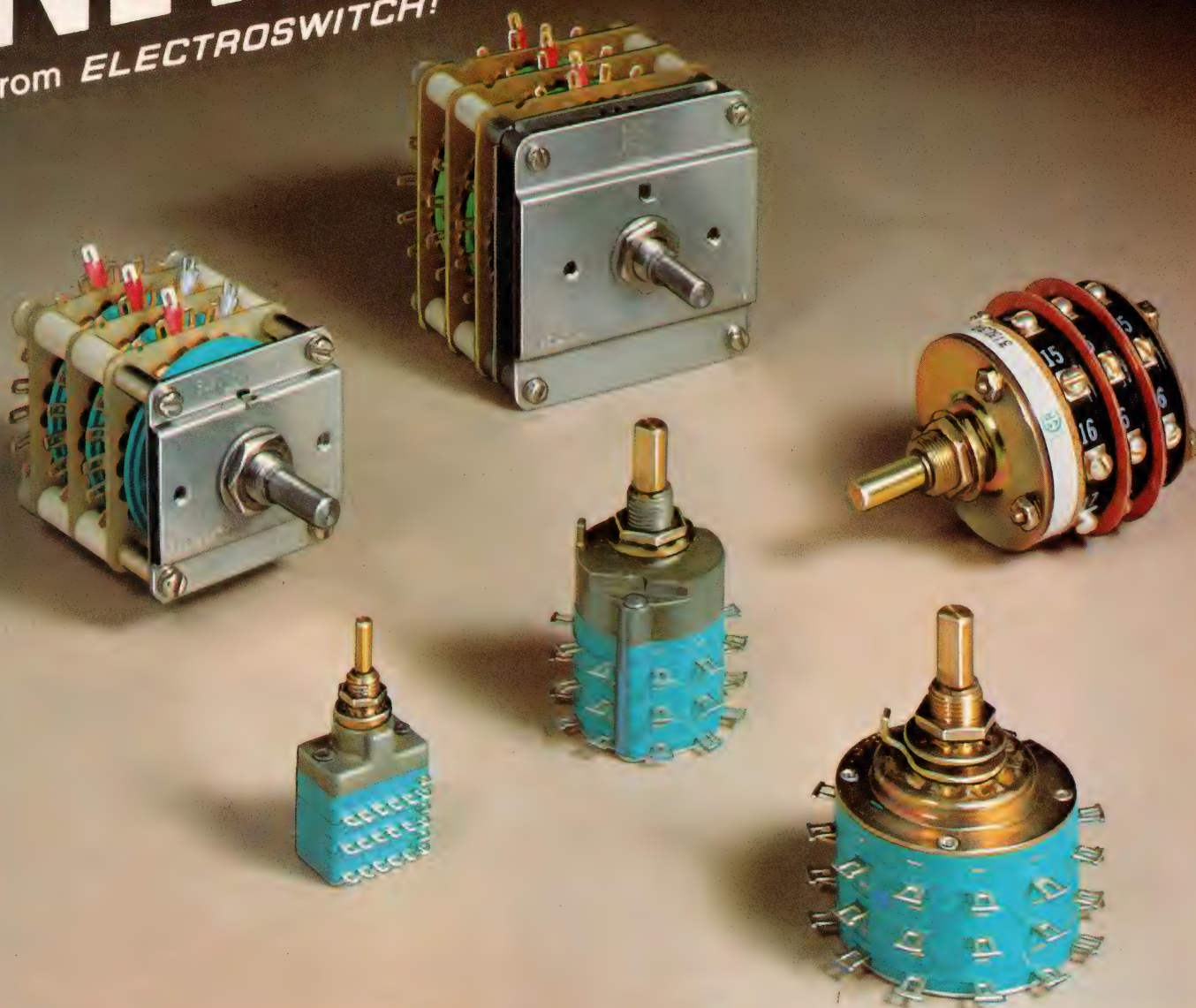
Bill Escovitz is an engineer at Hewlett-Packard Co (Colorado Springs, CO), where he designs oscilloscopes. He was previously employed by the University of Chicago. Bill holds a BA in physics from Dartmouth and MS and PhD degrees in physics from the University of Chicago. He is a member of the American Physical Society and the IEEE.



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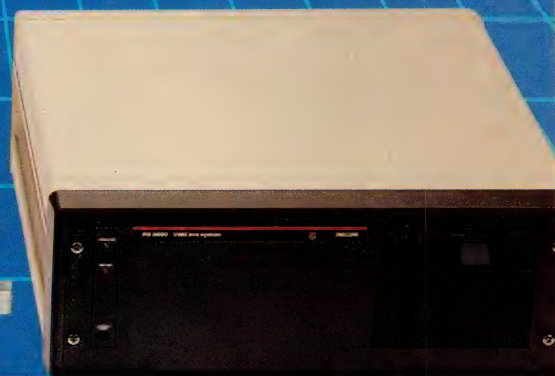
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DESIGN IDEAS

EDITED BY KEN MARRIN

Circuit provides temperature compensation

Joe Lutz

Peninsula Engineering, Redwood, CA

The circuit shown in **Fig 1** provides temperature compensation for a microwave amplifier circuit's gain and gives three degrees of freedom over the amplifier's operating temperature range (-40 to $+60^{\circ}\text{C}$). To provide compensation, the circuit sends a control signal to a pin diode that's in series with the amplifier's main signal path. As the current through the pin diode decreases, the diode provides more attenuation. As the current increases, the diode provides less attenuation.

Fig 2 shows the relationship between diode current and operating temperature. At room temperature, IC_{1b} and R_{10} supply a constant current of 0.16 mA to the diode. This current remains constant until the temperature falls to -10°C . At -10°C , IC_{1b} slowly begins to shut off. Finally, at -30°C , IC_{1b} supplies no current. At this temperature, the only current that the diode

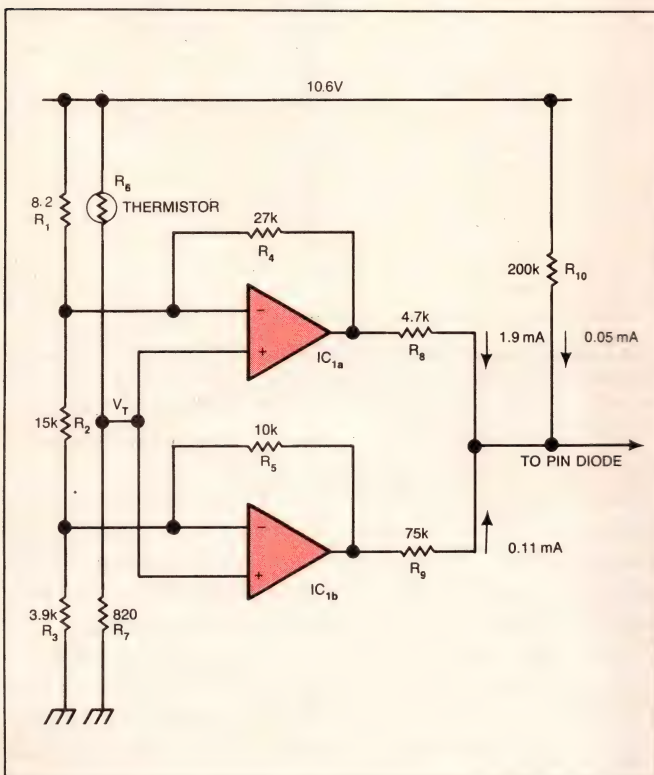


Fig 1—This circuit provides temperature compensation for a microwave amplifier circuit's gain. With the components shown, the circuit provides three degrees of freedom over -40 to $+60^{\circ}\text{C}$.

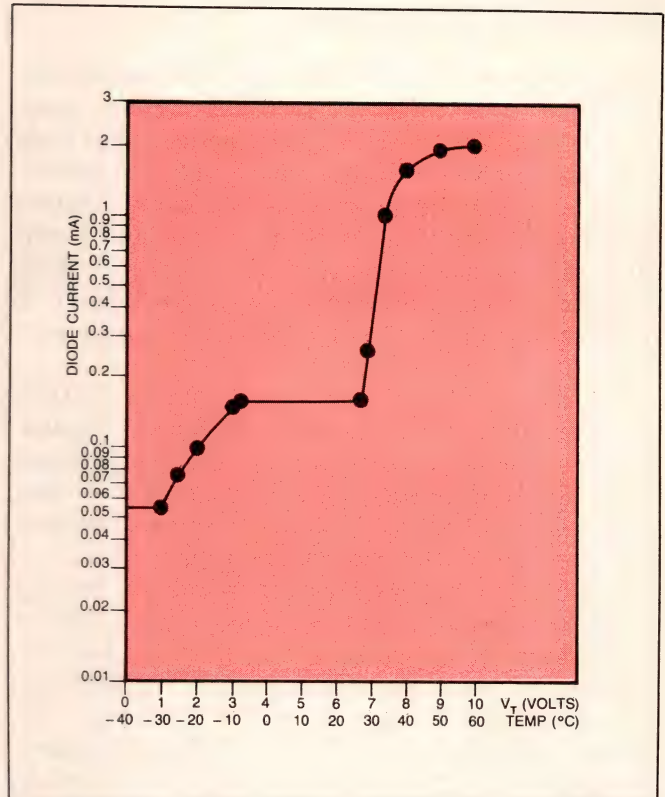


Fig 2—This graph shows the relationship between the system's operating temperature and the pin-diode current supplied by the compensation circuit in **Fig 1**. The control current that the compensation circuit supplies acts as a control signal to the pin diode, whose attenuation is proportional to the control current.

receives is the 0.05 mA provided by R_{10} . R_5 's value determines the temperature range over which this transition occurs.

For temperatures as high as 40°C , R_{10} and IC_{1b} provide a constant 0.16 mA . Above 40°C , however, IC_{1a} 's current output rises dramatically. At 55°C , IC_{1a} saturates, and the pin diode provides its maximum attenuation.

To modify the response shown in **Fig 2** for different applications, you can adjust either the feedback resistors (R_4 and R_5) or the reference voltage divider (determined by resistors R_1 , R_2 , and R_3). To give the circuit additional degrees of freedom, you can add more op amps.

EDN

To Vote For This Design, Circle No 745

PCM filter offers lowpass, bandpass options

David J Donovan
Harris Corp, Melbourne, FL

The Harris HC-5512, 5512A, and 5512C pulse-code-modulated (PCM) filters are switched-capacitor monolithic circuits that were originally designed for PCM codec filtering in systems that sample at 8 kHz. However, by taking advantage of the devices' receive lowpass filter and transmit highpass filter, you can build a wide range of lowpass and highpass filter circuits with cutoff frequencies ranging from 200 Hz to 10 kHz (Fig 1). To program the filter's cutoff frequency, you simply vary the device's input clock frequency.

The chip's transmit side uses a 200- to 3400-Hz bandpass filter, which comprises a fifth-order elliptical lowpass filter cascaded with a fourth-order highpass filter. The receive side uses a 3400-Hz lowpass filter with $\sin X/X$ correction. Second-order antialiasing filters precede both the transmit and receive filters.

To specify a 3-dB cutoff frequency, you first connect the chip's CLK_0 input (pin 14) to either V_{CC} , GND, or V_{BB} . (These connections result in internal clock frequencies of 2.048, 1.544, and 1.536 MHz, respectively.) V_{CC} 's and V_{BB} 's nominal values are +5V and -5V, respectively. You then set the filter's cutoff frequency by applying an external clock signal to pin 12, whose frequency lies between 300 kHz and 5 MHz (the device won't work at frequencies out of this range).

For a 300-kHz external clock frequency, the lowpass filter will have a cutoff frequency of 1 kHz, and the bandpass filter will have a lowpass cutoff frequency of 200 Hz and a highpass cutoff frequency of 1 kHz. At 5 MHz, the lowpass filter will have a cutoff frequency of 10 kHz, and the bandpass filter will have a lowpass cutoff frequency of 5800 Hz and a highpass cutoff frequency of 9 kHz.

Between 300 kHz and 5 MHz, the cutoff frequencies for both the lowpass and bandpass filters will vary nearly linearly with the programming frequency, with some compression occurring at either end of the programming frequency's spectrum. The bandpass filter's bandwidth will remain constant at 3200 Hz, except for some compression at the lower end of the programming spectrum. The least amount of compression will occur for the highest internal clock frequencies (ie, when pin 14 is connected to V_{CC}).

At 3300 Hz, the chip's receive filter provides an inherent gain. You can compensate for this gain by providing pole-zero compensation at the receive filter's

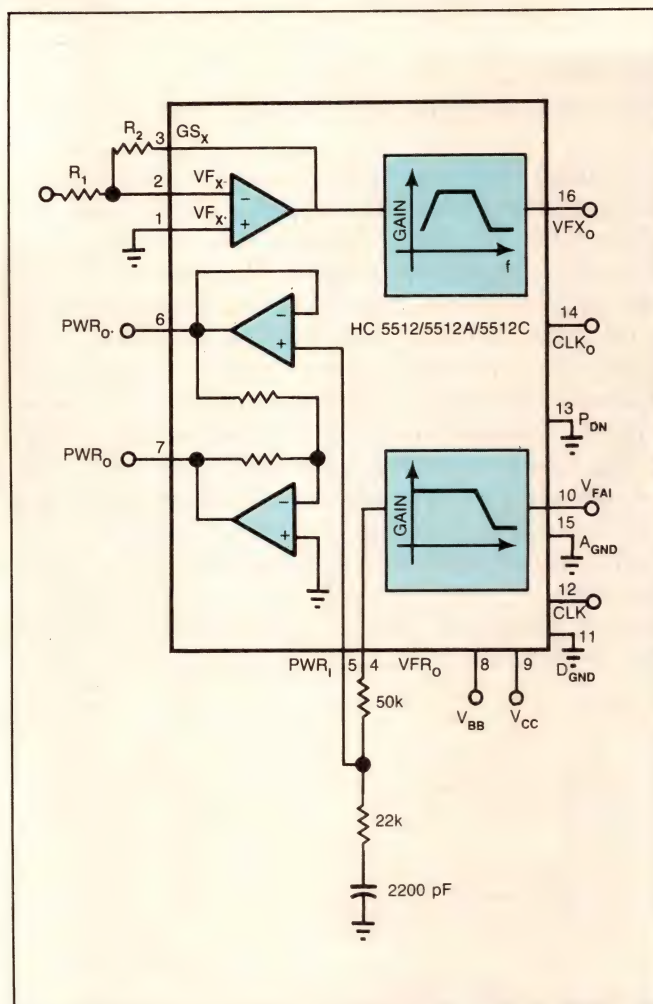


Fig 1—You can program this PCM filter to act as either a lowpass or highpass filter. By varying the chip's external clock frequency between 300 kHz and 5 MHz, you can select filter cut-off frequencies between 200 Hz and 10 kHz.

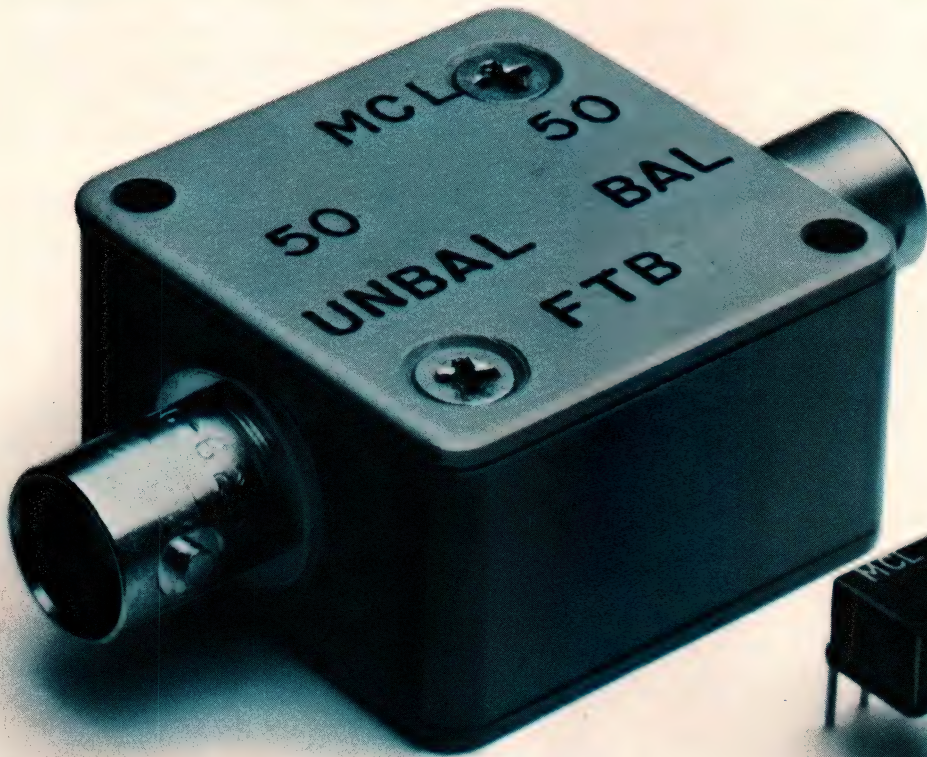
output. For the values shown in Fig 1, the chip uses a pole at 1 kHz and a zero at 3300 Hz to provide the compensation. The chip's transmit channel provides an inherent gain of 3 dB; you can increase this gain to as much as 20 dB by adjusting resistors R_1 and R_2 .

Both the transmit and receive outputs can drive a 3.2V p-p signal into a 10-k Ω , 25-pF load. The power-amp outputs, PWR_0^+ and PWR_0^- , can drive a 5V p-p signal into a 300 Ω single-ended load or a 10V p-p signal into a 600 Ω balanced load.

EDN

To Vote For This Design, Circle No 743

RF transformers

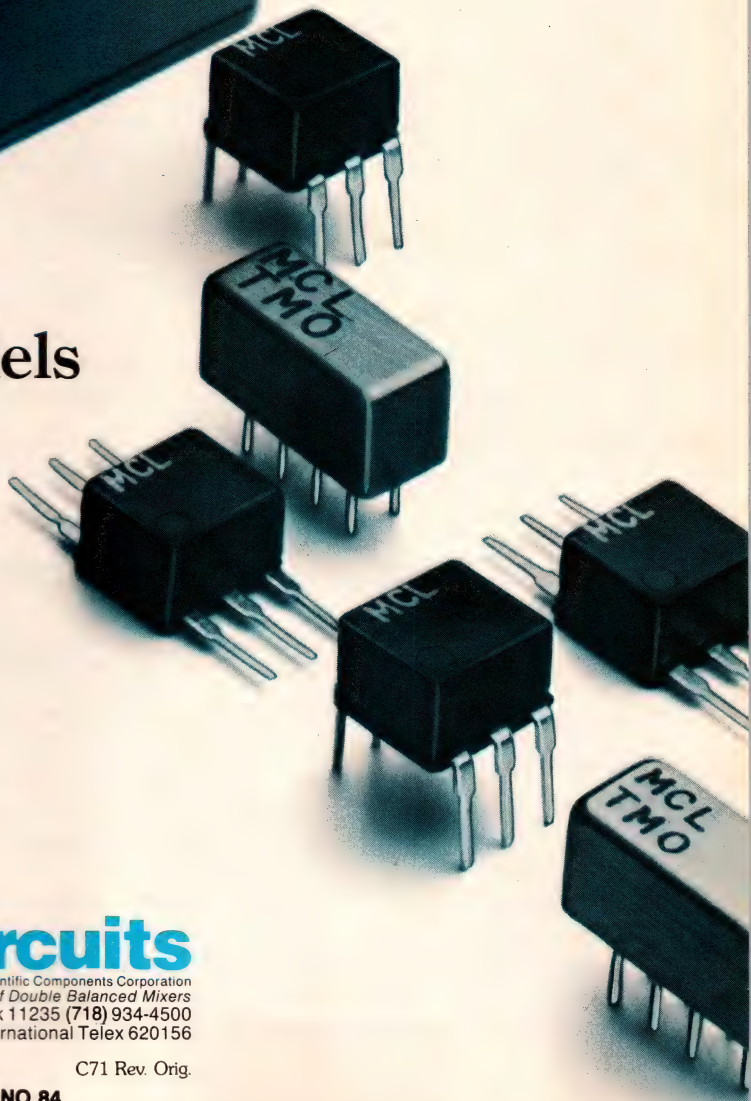


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Program provides gray/binary conversion

Dan G Sporea
Central Institute of Physics, Magurele, Romania

In position-encoder systems that use a μ P to handle data processing, the position encoder uses gray code and the μ P uses binary code to process the position

data. The programs in **Tables 1** and **2** convert binary to gray and gray to binary for the Z80 processor. The algorithms that the programs are based on are derived from the parallel-conversion hardware shown in **Fig 1**. The programs operate first on the word's most significant byte.

TABLE 1—BINARY TO GRAY CODE CONVERSION PROGRAM

3000	78		LD A,B	THE MOST SIGNIFICANT BYTE OF THE NUMBER TO BE CONVERTED
3001	08		EX AF,AF'	IS STORED.
3002	CB28		SRA B	THE MOST SIGNIFICANT BYTE IS SHIFTED RIGHT.
3004	08		EX AF,AF'	CONVERT THE LEAST SIGNIFICANT BIT OF THE NUMBER TO BE CONVERTED. STORE THE MOST SIGNIFICANT BYTE IN THE CARRY FLAG OF THE STATUS REGISTER F'.
3005	A8		XOR B	PART OF THE MOST SIGNIFICANT BYTE OF THE RESULT IS COMPUTED, EXCEPT FOR ITS MOST SIGNIFICANT BIT.
3006	CB78		BIT 7,B	THE MOST SIGNIFICANT BIT OF THE RESULT IS OBTAINED.
3008	47		LD B,A	LOAD THE RESULT'S MOST SIGNIFICANT BYTE IN REGISTER B.
3009	2007		JRNZ CNV 1	
300B	08	CNV 2	EX AF, AF'	THE CARRY FLAG CONTAINS THE LEAST SIGNIFICANT BIT OF THE MOST SIGNIFICANT BYTE OF THE NUMBER TO BE CONVERTED.
300C	79		LD A,C	THE ACCUMULATOR IS LOADED WITH THE SECOND BYTE OF THE NUMBER TO BE CONVERTED.
300D	CB19		RR C	THE SECOND BYTE'S MOST SIGNIFICANT BIT IS ROTATED. THE LEAST SIGNIFICANT BIT OF THE MOST SIGNIFICANT BYTE OF THE NUMBER TO BE CONVERTED IS INPUT FROM THE CARRY FLAG.
300F	A9		XOR C	THE LEAST SIGNIFICANT BYTE OF THE RESULT OF THE NUMBER TO BE CONVERTED IS COMPUTED.
3010	AF		LD C,A	STORE RESULT IN REGISTER C.
3011	C9		RET	RESULT IS STORED IN REGISTERS B AND C.
3012	CBF8	CNV1	SET 7,B	CORRECT THE RESULT'S MOST SIGNIFICANT BIT.
3014	18F5		JR CNV 2	

TABLE 2—GRAY CODE TO BINARY CONVERSION PROGRAM

3100	2610		LD H,10 H	LOAD THE LOOP COUNTER.
3102	7A		LD A,D	THE MOST SIGNIFICANT BYTE OF THE NUMBER TO BE CONVERTED IS LOADED IN THE ACCUMULATOR.
3103	CB07	CNV	RLC A	THE CARRY FLAG RECEIVES THE CURRENT BIT OF THE RESULT.
3105	CB11		RL C	THE CURRENT BIT OF THE RESULT IS SHIFTED IN RESULT REGISTERS B AND C, WITH THE MOST SIGNIFICANT BYTE STORED IN REGISTER B.
3107	CB10		RL B	
3109	CB0F		RRC A	THE MOST SIGNIFICANT BIT IN THE ACCUMULATOR IS RESTORED.
310B	CB23		SLA E	THE NUMBER TO BE CONVERTED IS ROTATED.
310D	CB12		RL D	
310F	AA		XOR D	THE CURRENT BIT OF THE RESULT IS COMPUTED.
3110	25		DEC H	DECREMENT LOOP COUNTER.
3111	20F0		JRNZ CNV	COMPUTE ALL BITS OF THE RESULT. STORE RESULT IN REGISTERS B AND C.
3113	C9		RET	

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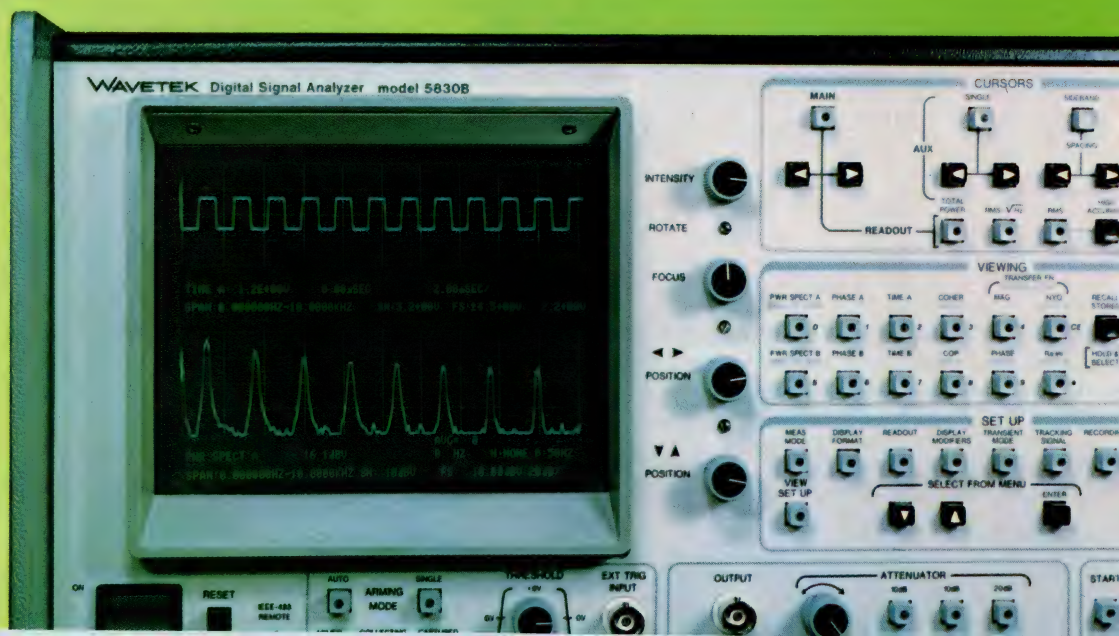
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DESIGN IDEAS

The program in **Table 1** converts binary code to gray code and is based on the hardware shown in **Fig 1a**. The program stores both the binary number that you're converting and the resulting gray number in registers B and C.

The program in **Table 2** converts gray code to binary code and is based on the hardware shown in **Fig 1b**. The program stores the gray number that you're converting in registers D and E. It stores the resulting binary number in registers B and C.

Both programs avoid time- and memory-consuming memory-addressing instructions by relying exclusively on the Z80's internal registers. The program also improves execution speed by taking advantage of the Z80's rotation and bit-manipulation instructions. **EDN**

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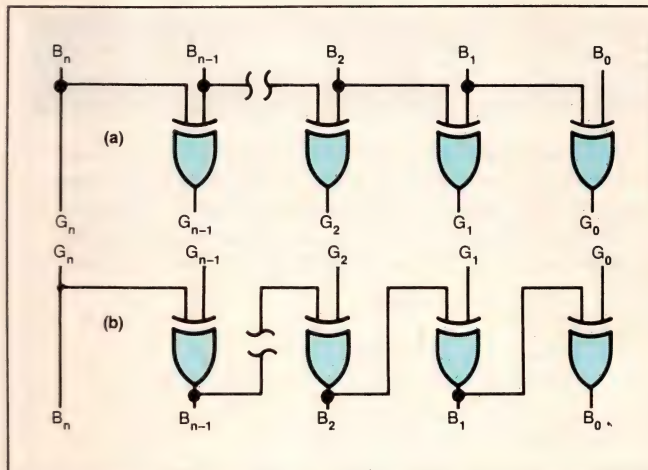


Fig 1—These binary-to-gray (a) and gray-to-binary (b) parallel-conversion devices serve as hardware models for the programs shown in Tables 1 and 2.

Vary frequency without changing duty cycle

Gordon Rogers
Bradenton, FL

In some pulse-generator applications, you may want to vary a pulse's frequency without changing its duty cycle. **Fig 1** shows you how to do this with a dual monostable multivibrator and a dual-gate MOSFET. R_1 and C_1 determine the pulse's frequency. R_2 determines the duty cycle. The sawtooth waveform at IC_{1A}'s pin 2 drives the FET, which in turn produces a sawtooth waveform with an adjustable dc component. R_2 's setting determines how much of the FET's output waveform triggers IC_{1B}. IC_{1A}'s Q₁ output resets IC_{1B}, which is

configured as a bistable multivibrator.

Output Q₂ of IC_{1B} goes high when the FET triggers pin 12 and goes low when IC_{1B} sends a reset pulse to pin 13. Because the trigger level applied to pin 12 is independent of frequency, the duty cycle is also independent of frequency. With the circuit values shown, you can vary the frequency between 8 and 50 Hz and the duty cycle between 3 and 97%. The frequency decreases by about 10% for duty cycles of 10 and 90%.

EDN

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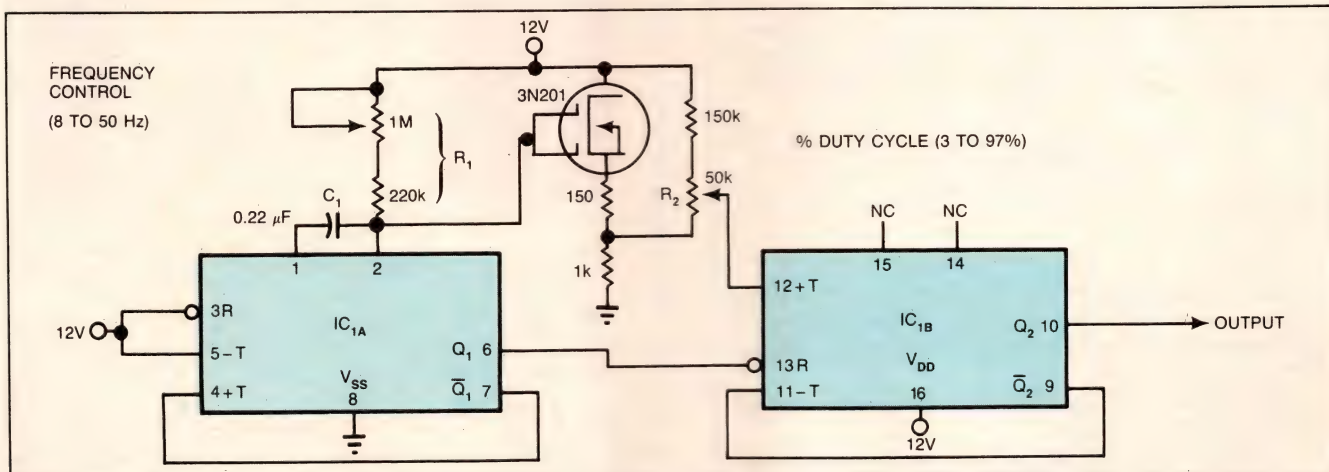


Fig 1—This circuit allows you to modify a pulse's frequency while keeping its duty cycle constant. By adjusting R_2 , you can select duty cycles from 3 to 97%.

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Circuit measures capacitor's resistance

Fred Brown

Consulting Engineer, Lake San Marcos, CA

To test large numbers of capacitors in production runs, use the circuit in **Fig 1a**, which lets you use an oscilloscope to determine a capacitor's series resistance at a glance. You drive the circuit with a square wave. If the capacitor has no series resistance, the oscilloscope will display a perfect sawtooth wave. If the capacitor has series resistance, however, the oscilloscope will display a sawtooth wave with a square wave superimposed on it (**Fig 1b**). The larger the superimposed square wave, the greater the series resistance.

To obtain a quick approximation of the capacitor's series resistance, look at the ratio of e_r to e_c . For $RC \gg T$, $e_c = ET \div RC$, where T is the square wave's period and e_c is the voltage across the capacitor. The ratio of e_r to e_c equals the ratio of the capacitor's series resistance to $T \div C$. For nonpolarized capacitors, you can omit the dc polarizing voltage.

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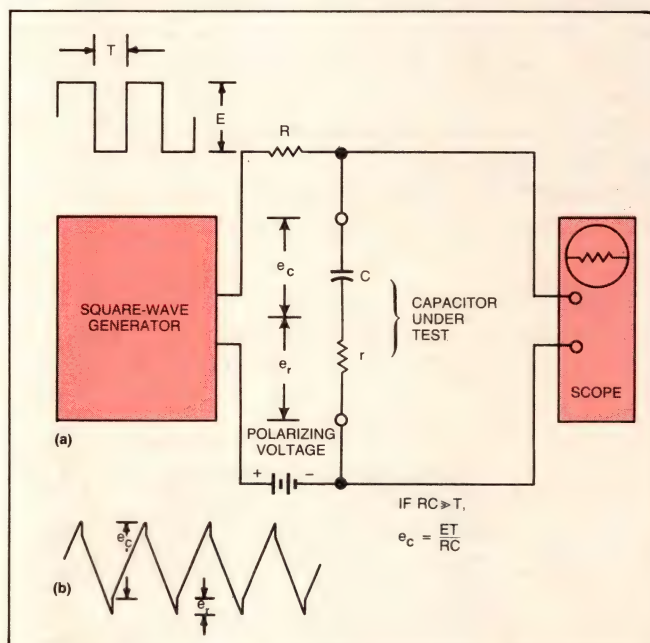


Fig 1—You can quickly determine a capacitor's series resistance by using the circuit in **a**. By looking at the relative magnitudes of e_r and e_c (**b**), you can decide whether the capacitor's resistance lies within acceptable limits.

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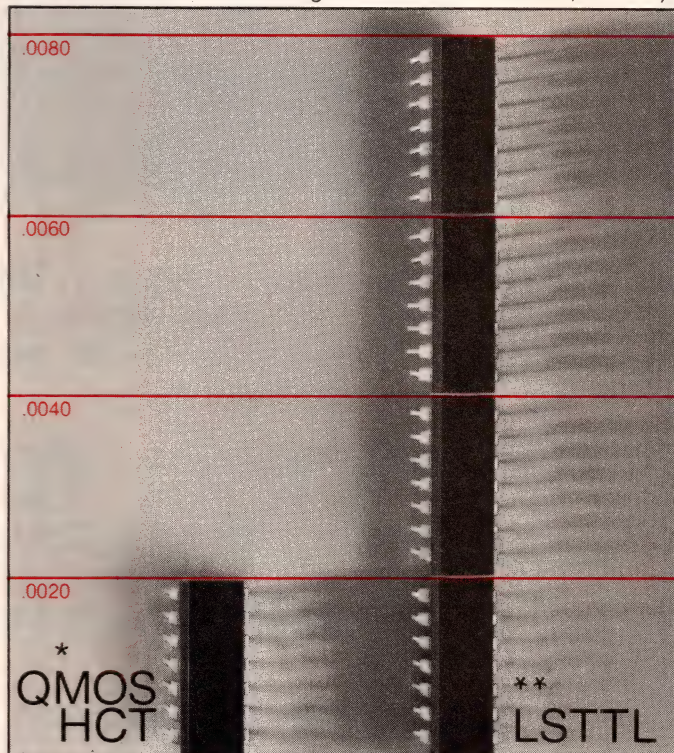
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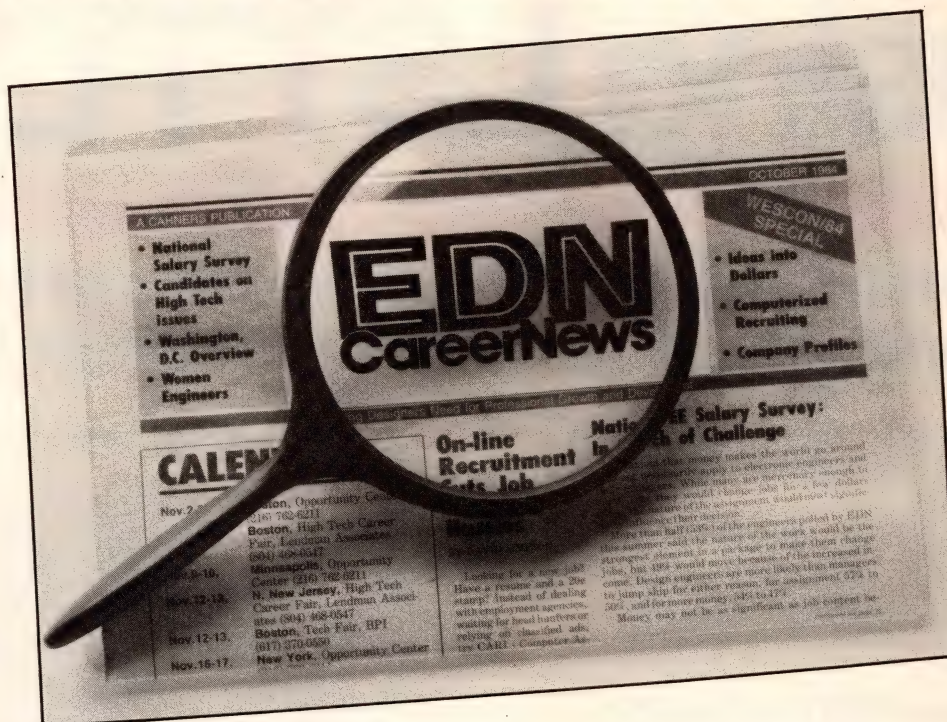
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Circle No 350



MICROWAVE/RF CAE

Version 1.3 of the Touchstone microwave/RF CAE program provides noise-figure analysis for as many as four stages of noise measurement and optimization. Analyses include shunt and series feedback, device parasitics, and ohmic losses in amplifier matching and feedback components. Version 1.3 also provides Monte Carlo yield predictions, including random variations of element values and wave-scattering data. The program reads this wave-scattering data into the HP 8510 network analyzer. The HP 8510 interacts with this CAE package,

over the IEEE-488 bus, on either an IBM PC (or PC compatible) with 640k bytes of RAM, or an HP 2000 Series computer with 1.25M bytes of RAM. The microwave/RF program calculates generalized scattering parameters based on frequency-dependent source and load impedances. In addition, the program features elements such as bipolar transistors, broadside-coupled lines in striplines, and a rectangular-waveguide terminator. Other capabilities include voltage-gain analysis for 2-port networks with 50 Ω or non-50 Ω source and load terminations, as well as exponential frequency sweeps for creating a common ratio between frequencies. \$7500.

Eesof Inc., 31194 LaBaya Dr., Suite 205, Westlake Village, CA 91362. Phone (818) 991-7530. TLX 384809.

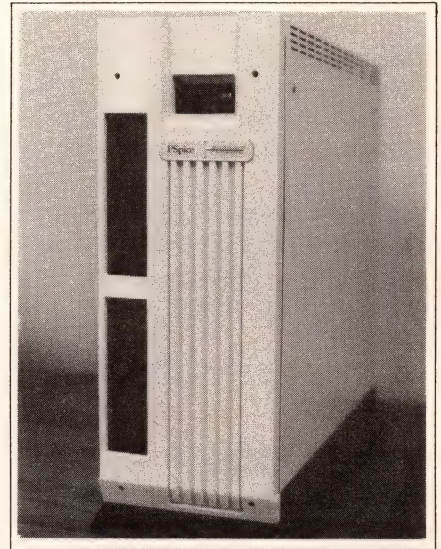
Circle No 351

3-D PERSPECTIVE

An added feature in VersaCAD Advanced software provides 3-D perspectives that you can rotate, edit, and use in other plots generated by the program. The software offers three drawing options: wire frame, which shows all the lines in the construction; backplane, which removes the back sides with a keystroke; and hidden line, which deletes backplane lines after calculating those that would be hidden from view. This CAD system includes 10 built-in primitives (arcs, French curves, and polygons); point-and-place symbol libraries; autodimensioning; proportional and unproportional scaling; and 250 overlay levels. Inquire and calculate functions evaluate area and perimeter totals, centers of gravity, cross-section areas, and moments of inertia. IGES compatibility is standard. \$1995.

T&W Systems Inc., 7372 Prince Dr., Suite 106, Huntington Beach, CA 92647. Phone (714) 847-9960.

Circle No 452



SPICE ACCELERATOR

PSpice Turbine accelerates the company's PSpice circuit-simulation program, permitting it to run on an IBM PC as fast as Spice runs on an unloaded VAX 11/780 running VMS with floating-point hardware. The device comes in a stand-alone chassis approximately the size of the PC chassis. It interfaces with a PC via a card that plugs into one of the short slots in a PC's backplane and a shielded ribbon cable that connects the card to the accelerator. Because the Fortran source code for the simulation program is included, users can write their own electrical-device equations. The accelerator can handle circuits containing as many as 200 transistors and routinely performs self-diagnostics during power-up. \$19,500.

Microsim Corp., 14101 Yorba St., Tustin, CA 92680. Phone (714) 731-8091.

Circle No 352

PRESENTATION PLOTS

Tutsim, a simulation program for modeling continuous systems on a μ C, can produce presentation-quality plots. The program generates pen-plotter output that labels the X and Y axes of curves and titles and dates each plot. Hard copy and CRT images can include these annotations. You can also simulate systems if you can define their processes

with differential equations. To create a model, you must enter block, structural, and variable parameters in single-line format. The program optimizes systems that are described by time-dependent equations or differential equations. It is available for use on IBM μ Cs. \$495.

Applied i, 200 California Ave, Palo Alto, CA 94306. Phone (415) 325-4800.

Circle No 353

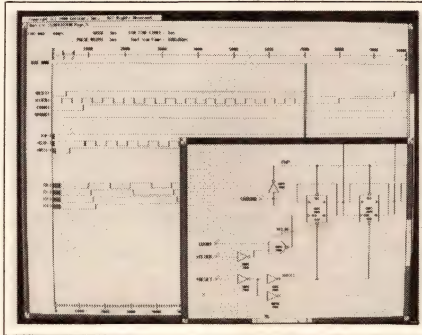
COLOR OPTION

This high-resolution color option is available for the CT1000 CAE design system. The software package supports the IBM enhanced color monitor and display adapter for the IBM PC, PC/XT, and PC/AT, providing 650x350-pixel resolution in 16 colors. You can define foreground and background colors, line widths, character fonts, and text placement. Based on a personal computer, the

CT1000 CAE design system supports the hierarchical Scald logic and timing verifier. CT1000 with color option, \$3750.

Case Technology Inc, 633 Menlo Ave, Menlo Park, CA 94025. Phone (415) 322-4057.

Circle No 354



IC DESIGN

The CDA 5000 CAE software package is available for Data General's Distributed System workstations as

well as for HP workstations. You can choose from two software packages: a schematic entry editor, which includes component libraries, and an event-driven logic and timing simulator. Schematic editor, \$19,900; simulator, \$15,000.

Cericor Inc, 716 E 4500 South, Salt Lake City, UT 84107. Phone (801) 264-8600.

Circle No 355

SCHEMATIC CAPTURE

When used with Designer III workstations, CAEPac II draws schematic diagrams. It features a schematic definition file (SDF), a schematic definition file compiler (SDFC), a schematic capture editor, and a net-list formatter. You can edit the SDF by using any text editor running under the Unix operating system and by defining all the schematic symbols and functional parameters. The schematic capture

This new solid state industrial timer lets you field-select from 4 operating modes and 8 timing ranges.

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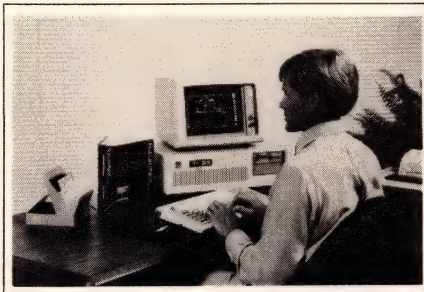
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editor operates in conjunction with the user-defined SDF to create a schematic diagram; it can automatically update an edited database. The net-list formatter offers the flexibility of C within a Unix environment. \$12,000.

Caeco, 2558 Mountain Industrial Blvd, Tucker, GA 30084. Phone (404) 493-7000. TWX 810-766-8099.

Circle No 356



TTL LIBRARY

This TTL parts library is available for Dash-Cadat, a logic simulator that runs on the IBM PC/XT or PC/AT. The library of primitives includes MOS and CMOS transistors and transmission gates; buffers and inverters; binary and BCD counters; encoders and decoders; 3-state drivers; and JK- and D-type flip flops and latches. The library also includes registers, transceivers, adders, ALUs, comparators, parity checkers, ROM, and RAM. Dash-Cadat requires that you add a 1M-byte 32016 processor board to the IBM PC. Dash-Cadat 40 is identical to Dash-Cadat, except that it replaces the 10M-byte Winchester disk drive on the PC/XT with a 40M-byte drive. Cadat-TTL library, \$1800.

Futurenet Corp, 6709 Independence Ave, Canoga Park, CA 91303. Phone (818) 700-0691. TWX 910-494-2681.

Circle No 357

VAX-BASED CAE

The CAE 2000 design-automation package runs on DEC's VAXstation I and VAX 8600. When running on a VAXstation, the software can oper-

ate as a stand-alone unit or as a node in a distributed-network environment for team engineering. It uses DEC's VMS Release 4 and DEC-shell. The package features schematic capture, logic simulation, circuit simulation, timing verification, and interfaces to other design tools. The VAX 8600 specs 4.2 times the speed of the 11/780, which, in turn,

affects the speed of the CAE package. Prices depend on applications: \$22,000 to \$50,000 for VAXstation package; from \$124,000 for the VAX 8600 tool. Shipments to begin in July.

CAE Systems Inc, 1333 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 745-1440.

Circle No 358

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Interactive Streamer
Ethernet™
Multiuser
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Minibox—Heurikon's new multi-user, multitasking workstation—puts the power of the MC 68000/68010 microprocessor (8 or 10 Mhz) and the flexibility of UNIX all in 1.5 square feet of desk space. Designed with the OEM in mind, Minibox gives you these features and capabilities you've been searching for: Electronic mail • Interprocess communications (IPC) • Fully integrated streaming tape drive, up to 280 MB of Winchester storage • 1 MB floppy drive • UNIX System V or III • Ethernet (TCP/IP) for fast expansion and networking • Floating Point Processor • CPM Shell for CP/M-to-UNIX link • Hotline customer support.

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Wisconsin 608 271 8700 Telex 469532

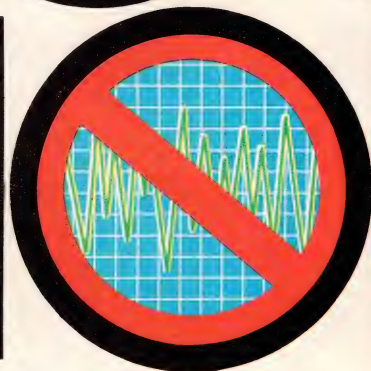
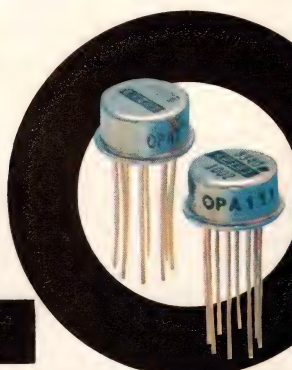
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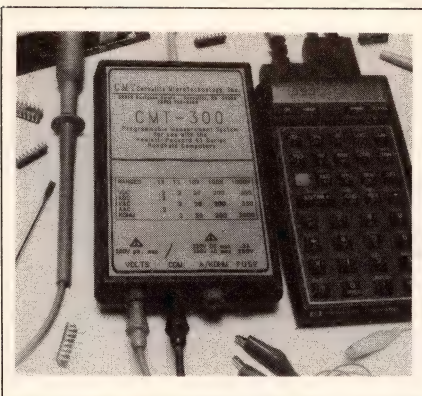
All parameters, including noise, 100% tested and guaranteed.

MODEL	NOISE (10kHz, max)	V _{os} (max)	DRIFT (max)	I _B (max)
OPA111BM	8nV/ $\sqrt{\text{Hz}}$	$\pm 250\mu\text{V}$	$\pm 1\mu\text{V}/^\circ\text{C}$	$\pm 1\text{pA}$
OPA27AJ	3.8nV/ $\sqrt{\text{Hz}}$	$\pm 25\mu\text{V}$	$\pm 0.6\mu\text{V}/^\circ\text{C}$	$\pm 40\text{nA}$



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MEASUREMENT SYSTEM

The CMT-300 is a portable, programmable measurement system that you can customize to operate with various transducers so it can measure temperature, moisture, light intensity, rpm, pH, and other physical conditions. For signal-analysis and data-reduction applications, you can connect the CMT-300 to an HP-41 handheld computer. The CMT-300 uses dual-slope integration to provide 3½-digit resolution in measuring dc and true-rms ac voltages, dc and true-rms current, and resistance. Programs in the CMT-300 allow you to use the device as a data logger, digital multimeter, and data-analysis tool. The product includes a keyboard overlay for the HP-41 and test leads. Optional accessories include the CMT-200, which can control external devices. CMT-300, \$350; CMT-341CX (includes HP-41CX), \$595.

Corvallis Microtechnology Inc., 33815 Eastgate Circle, Corvallis, OR 97333. Phone (503) 752-5456.

Circle No 359

FAULT TOLERANCE

Mimic Master provides redundant processing on one of its manufacturer's local-area networks to ensure continuous network operation in the event of the failure of a hard disk or master computer. Using software that emulates a fault-tolerant mode, the device duplicates, in real time, all data written to the network's master. When it detects the absence of the master computer, it acts as the network's primary computer,

thereby allowing maintenance personnel to locate and repair failed system components while the network continues to operate fully. It can support a network of as many as 63 stand-alone personal computers, running any combination of CP/M-80, CP/M-86, MS-DOS, or PC-DOS. Additional hard-disk storage and streaming-tape backup systems are available. From \$7950.

Digital Microsystems Inc., 1755 Embarcadero, Oakland, CA 94606. Phone (415) 532-3686.

Circle No 360



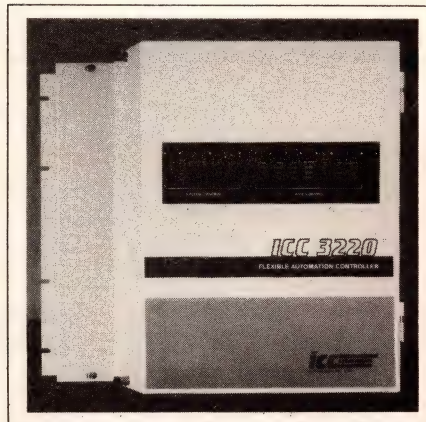
BROADBAND GATEWAY

This gateway server, the GS/6, lets you interconnect multiple Ethernet networks over CATV-based broadband networks. It facilitates the routing of data communication among as many as 255 Ethernet LANs over one 6-MHz broadband channel. By using a CSMA device, the server achieves signaling rates as fast as 2M bps. The server is suitable for organizations with multiple buildings. According to the manufacturer, this hybrid allows users to take advantage of Ethernet's high speed, low cost, and simple installation and maintenance. The server uses a mid- or high-split single-cable system (which fits on the spare channels of most installed cable) and such standard CATV-based broadband components as frequency translators. An Ethernet controller card and a 68000-based CPU card execute the XNS protocols. An HDLC controller card provides CSMA and address recognition for the data stream being fed into the server's FSK-based RF modem. Network traffic is filtered

so that a message is sent only to the address for which it is intended. \$10,500; annual license fee for routing software, \$150. Delivery, 60 days ARO.

Bridge Communications Inc., 1345 Shorebird Way, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 361



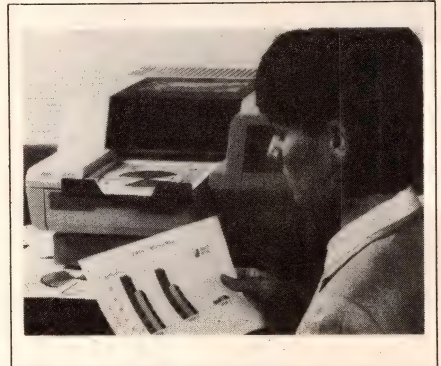
AUTOMATION CONTROL

The ICC 3220 automation controller features software packages for robotic control, machine control, and automated work cells; it can interface with CAD/CAM systems, factory computers, and factory networks. According to the manufacturer, the controller combines the power of an industrial computer, the flexibility of a programmable logic controller, and as many as eight axes of closed-loop brushless servo control. Because the controller offers direct numerical processing, users can select the parameters for either dc or brushless servos. The processing system uses 16-bit μ Ps with real-time adaptive algorithms rather than the usual analog and digital hardware. By using this software approach to automation control, the device does not require analog signal-processing components such as Hall-Effect sensors, tachometers, and optical encoders. \$8600 to \$24,000.

International Cybernetics Corp., 105 Delta Dr, Pittsburgh, PA 15238. Phone (412) 963-1444.

Circle No 362

COMPUTERS & PERIPHERALS



GRAPHICS PRINTER

Combining color printing and graphics processing in one machine, the LCP01 printer contains the company's J-11 μ P and page-buffer memory, which relieve the host computer of the graphics-processing operation. This ink-jet printer produces an image on either $8\frac{1}{2} \times 11$ -in. or A4 ($8\frac{1}{4} \times 11\frac{1}{4}$ -in.) paper in approximately 2 min. Resolution is 154 dots/in. both horizontally and vertically. Connected via a standard serial-line interface, the printer feeds, processes, and stacks as many as 100 sheets of paper or 50 transparencies automatically. The printer creates images in eight highly saturated colors and as many as 216 shades. Operating noise is <58 dBA. The office-size printer includes self-test diagnostics. \$14,595.

Digital Equipment Corp., 146 Main St., Maynard, MA 01754. Phone (800) 344-4825.

Circle No 363



BUSINESS SYSTEM

This version of the DECmate II business computer, the Omnimate, is a 3-user system in its standard configuration. It provides each user with access to WPS8, COS310, or OS/8 operating systems in a multi-

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DEVICE TYPE	MAXIMUM REVERSE RECOVERY TIME T_{RR}	PEAK INVERSE VOLTAGE PIV	AVERAGE CURRENT $I_O @ 55^{\circ}\text{C}$	MAXIMUM REVERSE CURRENT $I_R @ PIV @ 25^{\circ}\text{C}$
SERIES	(NSEC)	(VOLTS)	(mA)	(μA)
SHM-UF	60	1500-10,000	250-100	1.0
SHM-F	150	1500-10,000	250-100	1.0
SHM	5000	1500-10,000	250-100	1.0



Solid State Devices, Inc., 14830 Valley View Ave., La Mirada, CA 90638

CIRCLE NO 93



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CIRCLE NO 145

tasking environment. The computer features an HD-6120 μ P with 128k words of memory (expandable to 256k words), six serial ports, SCSI interface, BCD arithmetic, real-time clock and calendar, two 5¼-in. floppy-disk drives (1M byte each), and one 5¼-in. Winchester disk drive (40M bytes). The system also includes a VT220 word-processing terminal and a 180-cps draft-quality printer. Options include 10 serial ports that accommodate seven devices. \$9450.

Computer Extension Systems Inc., 17511 El Camino Real, Houston, TX 77058. Phone (713) 488-8830. TLX 774279.

Circle No 364

VIDEO PRINTER

This video photography system includes the Model 1600 video printer and the Model 250 video digitizer board, which performs frame grabbing via software. The 1600 produces television-quality color prints on plain paper without liquid chemicals or paper toners. With this system, you can access a video frame

from an IBM PC or a PC-compatible system and combine computer-generated graphics with captured video images. The 250 can capture a simple picture from a video signal in 1/60 sec. Offering a resolution of 256 pixels $\times$ 256 lines with four bits per color, the digitizer board captures red, green, and blue signals simultaneously; if you use a monochrome

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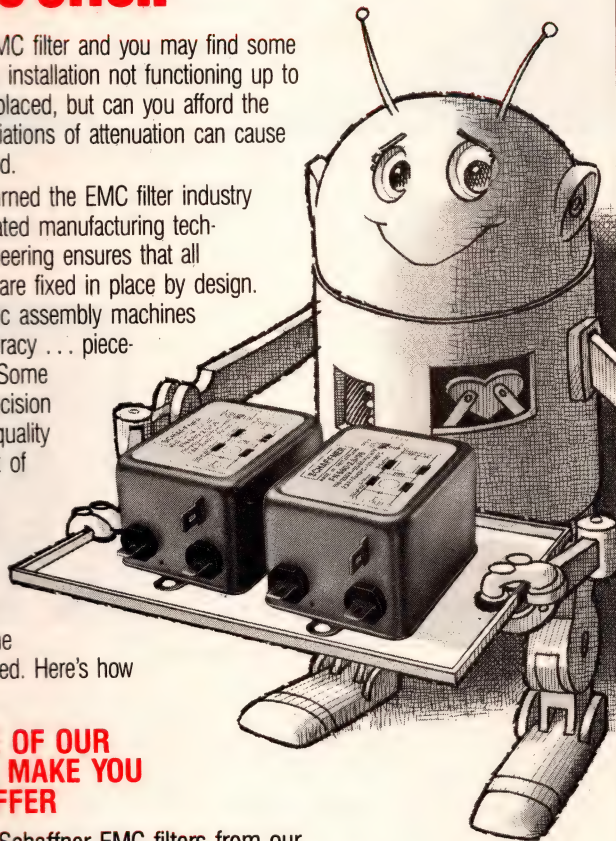
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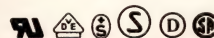
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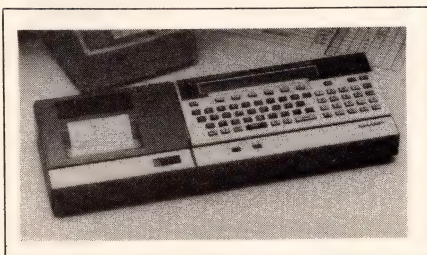
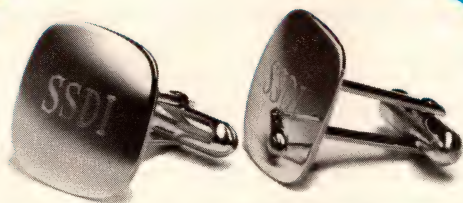


CHART COMPUTER

The Instant SPC with an updated variable chart program is a Sharp PC-1500A with additional preprogramming for plotting and printing in four colors. The device computes control limits; plots $\bar{X}/R$ charts; draws histograms; and calculates standard deviations, capability ratios, capability index, and the number of standard deviations from the average. The computer also calculates percentages over spec, prints additional copies, draws normal distribution curves, and plots as many as 60 averages or ranges. Four 1.5V AA batteries, ac adapter, cassette-recorder adapter cables, three rolls of printer paper, eight replacement pens, program and computer instruction manuals, and a case are included. \$995.

Elco Industries Inc., Rockford Div, Box 7009, Rockford, IL 61125. Phone (815) 397-5151. TWX 910-631-3420.

Circle No 365



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DEVICE TYPE	MAXIMUM REVERSE RECOVERY TIME T _{RR}	PEAK INVERSE VOLTAGE PIV	AVERAGE CURRENT I _O @ 55°C	MAXIMUM REVERSE CURRENT I _R @ PIV @ 25°C
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SHB-UF	60	1500-10,000	80-25	0.1
SHB-F	150	1500-10,000	80-25	0.1
SHB	5000	1500-10,000	80-25	0.1



Solid State Devices, Inc., 14830 Valley View Ave., La Mirada, CA 90638

CIRCLE NO 95

"Our NHS partnership saved a dying Oakland neighborhood."

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In 1975, there were 250 vacant or abandoned homes in Oakland's Elmhurst area. The neighborhood was dying. Then Neighborhood Housing Services, a non-profit partnership of residents, businessmen and local government was formed to help residents rehabilitate their homes. Now, 80% of the neighborhood's blighting influences have been eliminated. For every \$1 donated to the Oakland NHS for local operating support, \$39 has been reinvested in the neighborhood



by residents, financial institutions and city government NHS is succeeding in 136 cities. It needs the help of business leaders like us to continue its good work."

You can help. Call toll-free (800) 344-6472, or write Neighborhood Housing Services of America, 1951 Webster Street, Oakland, CA 94612.



Local partnership: key to neighborhood renewal



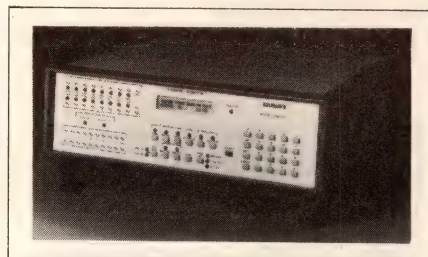
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COMPUTERS & PERIPHERALS

monitor, you can write to all three color planes simultaneously. The printer features an 8×10-in. editing area. A thermal printing head and color dye sheets provide hard-copy reproductions with over 4000 hues. Using a menu, you can adjust color contrast levels, choose positive or negative prints, and format copy. Color printer with Centronics-compatible interface, \$6500; digitizer board, \$1100.

Biflyx, 2522 Dupont Dr, Irvine, CA 92715. Phone (714) 476-3153.

Circle No 366



CHANNEL MONITOR

The Model DW300 monitors the IBM 370 and 4341 and equivalent compatible computer channels. This portable diagnostic machine provides multilevel triggering to pinpoint problems in situations where different makes and/or models of computer equipment are used. Connected to the IBM channel via bus and tag cables, the monitor features a library of such standard channel protocols as start I/O and interface disconnect. Using the hexadecimal keypad, you can program the monitor's line states to zero, one, or don't care. The unit captures as much as 8k bytes of data to aid in diagnostics and features a 40-character LCD plus controls for voltage and skew settings. The monitor records 8192 channel events for all 34 lines (tag, bus, and parity) at rates to 16 MHz. Triggers are based on any combination of line states or external events plus standard IBM sequences. LEDs indicate parity errors and the state of each tag line while the LCD shows the contents of the data bus in hex. Also displayed are the cur-

rent buffer location and a time stamp for each data point. An optional RS-232C card for operating an external printer, terminal, or modem is available. \$9450; RS-232C card, \$395.

Dataware Development Inc., 4204 Sorrento Valley Blvd, San Diego, CA 92121. Phone (619) 453-7660. TWX 910-335-2066.

Circle No 367

SUPERMINICOMPUTER

The 3260MPS is a tightly coupled superminicomputer that can contain a combination of as many as nine auxiliary processing units (APUs) and I/O processors in addition to its CPU. The system is asymmetric so each processor performs a primary function, and each has equal access to memory for data sharing and programs. The computer offers transparent parallel processing under OS/32, the company's Series



3200 operating system. Performance ranges from 1.2 MIPS in a configuration consisting of the CPU with one I/O processor to 7.2 MIPS in a fully expanded 9-APU system. Floating-point processors are standard in all processing units except the I/O processors. The task-scheduling microcode, in conjunction with cache memory for each processor, minimizes software overhead and reduces bus contention. The global memory bus specs a 64M-byte/sec bandwidth. Four versions are available including Model 3262-01, which provides a 2M-byte (2-bank) memory, an I/O processor with bus switches, and two DMA channels; and Model 3262-10, which features a

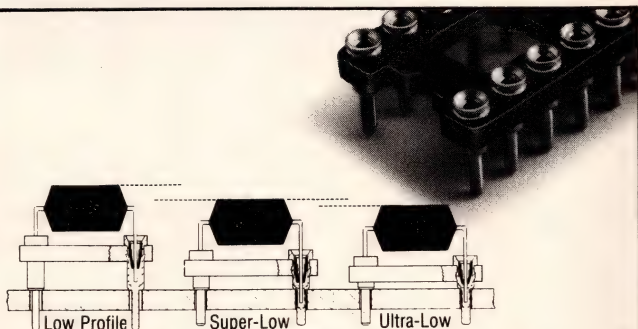
4M-byte (4-bank) memory, an APU, and four DMA channels. The computers are packaged in two 56-in. cabinets with power supplies and ac distribution panels. You can add APUs, I/O processors, memory and banks, DMA channels, I/O chassis and controllers, peripheral devices, and cabinets as needed. From \$185,000.

Perkin-Elmer Corp., Data Systems Group, 2 Crescent Pl, Oceanport, NJ 07757. Phone (201) 530-5900.

Circle No 368

3-SPEED MODEM

The CDS224 is a single-card, rack-mountable, 3-speed modem for asynchronous operation at 300 bps and asynchronous or synchronous operation at 1200 and 2400 bps. Suitable for the needs of a central communications facility, it features speed-sensing and autoanswer ca-



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CIRCLE NO 96

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Chromafilter is a high-resolution, contrast-enhancing, glare-reducing, abrasion-resistant polycarbonate or acrylic window material for all types of displays: LED, LCD, VFD, CRT, plasma, or electroluminescent. Available in sheets or fully fabricated, screen printed, and ready to use, in clear, neutral gray, or a wide variety of standard colors. Whatever the display, count on Chromafilter!



PanelGraphic Corporation
10 Henderson Drive, West Caldwell, New Jersey 07006
Phone (800) 222-0618 • In N.J. (800) 222-0617
TWX: 710-734-4367

CIRCLE NO 97

NEW! 2 AMPERE HIGH CURRENT HIGH VOLTAGE EPOXY RECTIFIERS. ULTRA-FAST, FAST, STANDARD.

Ratings to 2 Amps. Solid silver leads. + 150°C operating. Metallurgically bonded junctions. Industrial/military quality. Screening to TX or TXV level available. Applications: Lasers, HV power supplies, Radar Applications, HV multipliers. For free samples and pricing, call (213) 921-9660. TWX 910-583-4809.

DEVICE TYPE	MAXIMUM REVERSE RECOVERY TIME T _{RR} (NSEC)	PEAK INVERSE VOLTAGE PIV (VOLTS)	AVERAGE CURRENT I _O @ 55°C (mA)	MAXIMUM REVERSE CURRENT I _R @ PIV @ 25°C (uA)
SHE-UF	60	1500-10,000	1000-400	1.0
SHE-F	150	1500-10,000	1500-500	1.0
SHE	5000	1500-10,000	2000-600	1.0



Solid State Devices, Inc., 14830 Valley View Ave., La Mirada, CA 90638

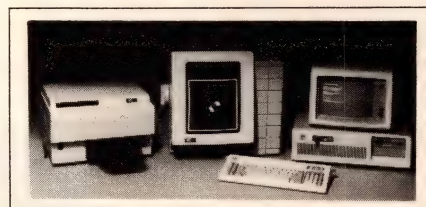
CIRCLE NO 98

COMPUTERS & PERIPHERALS

pabilities that automatically adjust the unit to the speed of each incoming call. Thus all users can access the central site using the same phone line and any modem. This feature in the 1200- and 2400-bps modes compensates for line interference and allows maximum data throughput even on marginal lines, according to the manufacturer. Optional autodial allows automatic dialing to remote sites. Integral diagnostics include digital self-test, analog self-test, and an internal-pattern generator and checker. From \$855.

Concord Data Systems Inc, 303 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-1394. TLX 951793.

Circle No 369



LASER PRINTER

Providing a resolution of 300×300 dots, Model CDS 2300's 1.28M-byte RAM stores a bit map of an 8½×11-in. page. The laser printer connects to most personal computers through a serial or Centronics port and offers four print formats: Diablo-630 emulation, Tektronix-4014 emulation, ANSI X3.64, and full bit-map image mode. For this last mode, the company offers a letter-quality type font in 10-pt normal, bold, or italics. You can space characters singly, proportionally, or independently on the page. The printer's controller uses an 8-MHz 80186 μ P and contains 1.28M bytes of bit-map RAM, 128k bytes of system RAM, and 128k bytes of system ROM. The system prints at a rate of 8 pgs/min. \$5695.

Corporate Data Sciences Inc, 2560 Mission College Blvd, Suite 102, Santa Clara, CA 95054. Phone (408) 980-9747. TLX 757453.

Circle No 370

SUPER POWER!

High reliability ELCOM® brushless DC servo motors are ideally suited to continuous process applications as well as demanding motion control functions in automated equipment. Optional, integrally mounted optical encoders facilitate use with latest digital control

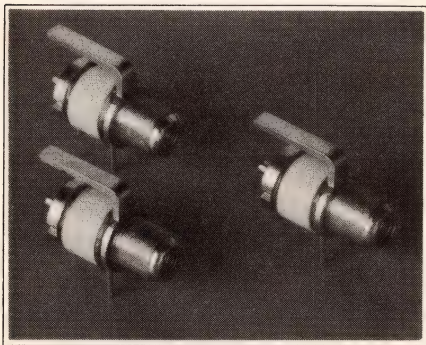
systems. Now available in 3 frame sizes and multiple lengths up to 50mm square x 100.4mm long; Continuous duty outputs to 47 oz.-in. at 7,200 rpm (1/3 hp). For complete information on how ELCOM® brushless motors can improve your design, call PITTMAN at (215) 256-6601.

PITTMAN®
HARLEYSVILLE, PA 19438-0003 USA
A DIVISION OF PENN ENGINEERING & MANUFACTURING CORP

CIRCLE NO 99

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NEW PRODUCTS: COMPONENTS & PACKAGING



TRIM CAPACITORS

The C-Line 14-turn air-dielectric trimming capacitors have high Q and high resolution. Specifications include a Q at 100 MHz of 1000 min, a capacity range of 2 to 7 pF, and a resolution of 0.4 pF/turn. The units measure 0.305×0.697 in., with three mounting styles available. \$0.85 (1000). Delivery, 6 to 8 wks ARO.

Murata Erie North America Inc., 1148 Franklin Rd SE, Marietta, GA 30067. Phone (404) 688-4181.

Circle No 371

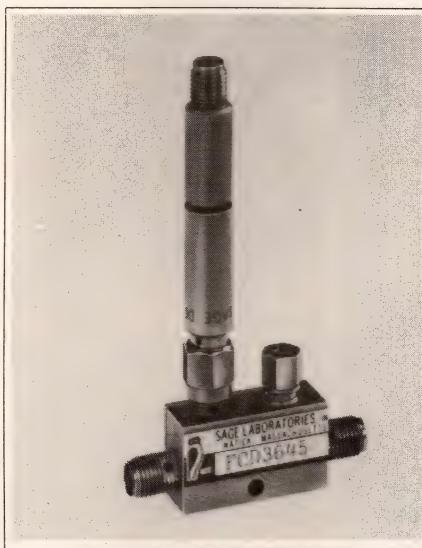
SIGNALING COMPONENTS

The 3501 multifrequency generator and the 3101 multifrequency receiver are signaling components for telecommunications. The generator, which meets Bell MF and CCITT specifications, contains a CMOS digital-frequency synthesizer, a D/A converter, and filtering circuitry. A 2.976-MHz crystal generates 18 frequencies for multifrequency interoffice signaling. In each signaling format, six frequencies provide 15 tone combinations. Starting sine waves at 0° phase permit control of harmonic content. Suitable for use with the US RI or European CCITT No 5 signaling formats, the receiver detects pulses, transfers the digital information to control equipment, and establishes connections through the switches. A 2.976-MHz external crystal determines the frequencies and the timing for detection. The unit consists of six internal band-pass filters and limiters as well as a monolithic decoder. Six data outputs indicate the individual tones

received; the seventh indicates a valid 2-of-6 code; and the eighth warns that an improper tone combination has been received. Generator, \$46; receiver, \$214.50 (500). Delivery, 4 to 6 wks ARO for prototypes.

Tektronix Inc., Box 500, Beaverton, OR 97077. Phone (503) 627-4220.

Circle No 372



COUPLER/DETECTOR

Model FCD3645, an X-K band coupler/detector, operates over 7.5 to 17 GHz. Input VSWR is 1.5:1 max, 1.2:1 typ. The device specs an insertion loss of <1 dB. Video output voltage, with 100 mA bias and 0 dBm RF input power, is 5 mV min, 25 mV typ. \$600. Delivery, 60 to 90 days ARO.

Sage Laboratories Inc., 3 Huron Dr, Natick, MA 01760. Phone (617) 653-0844.

Circle No 373

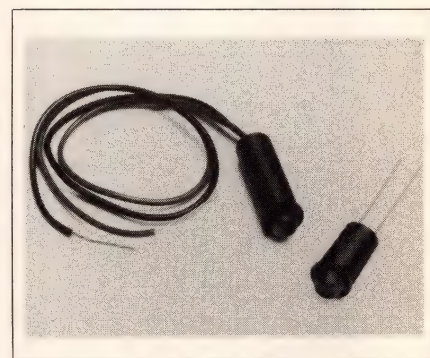
ISOLATION AMPLIFIER

The AD295 hybrid isolation amplifier combines $\pm 2500V$ isolation with maximum nonlinearity of $\pm 0.012\%$. Two internal transformers provide 3-port isolation among the input, output, and power-supply ports. Isolated power for signal-conditioning circuitry is rated at $\pm 15V$ dc at 5 mA, thus eliminating the need for

an external dc/dc converter. You can configure the input amplifier as a buffer, inverter, subtractor, or differential amplifier. And you can program the gain from 1 to 1000 V/V at the input or output stages (or both). Input noise equals 2 μV p-p, and common-mode rejection is 106 dB. The isolation amplifier is available in three grades, offering different tolerances of nonlinearity, offset voltage drift, and input offset drift. Key specifications include $\pm 1.5\%$ gain accuracy typ, ± 60 ppm/°C gain drift, ± 18 mV output offset voltage, and ± 3 mV maximum input offset voltage. \$78.75 to \$101.25 (100).

Analog Devices Inc., Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 374



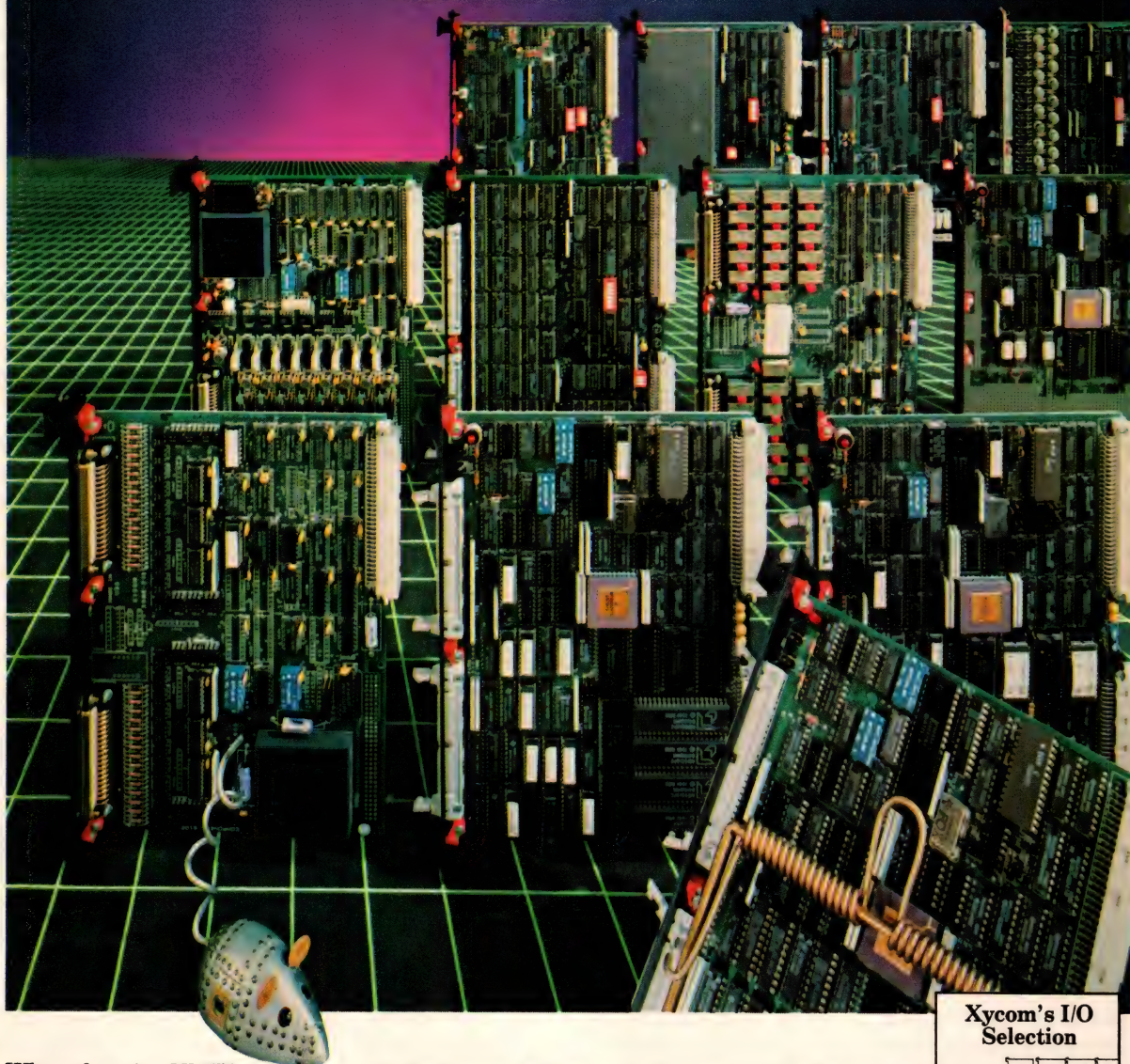
LEDs

P407 Series LEDs have a medium-profile lens (0.15-in. protrusion above the panel surface) and come in three colors (red, amber, and green). Choices for mounting include snap-in mounting (in a ¼-in. panel cutout) with fixed leads and snap-in mounting with 6-in. flying leads. The LEDs can be specified with a built-in resistor for operation ranging from 2.4 to 24V dc. They can also be driven by an ac source below 15V. For ac operation above 15V, you'll need an external rectifier. \$0.35 (1000). Delivery, stock to 5 wks ARO.

Data Display Products, 301 Coral Circle, El Segundo, CA 90245. Phone (800) 421-6815; in CA, (213) 640-0442.

Circle No 375

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in designing and manufacturing industrial microcomputers.

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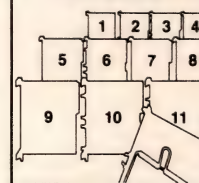


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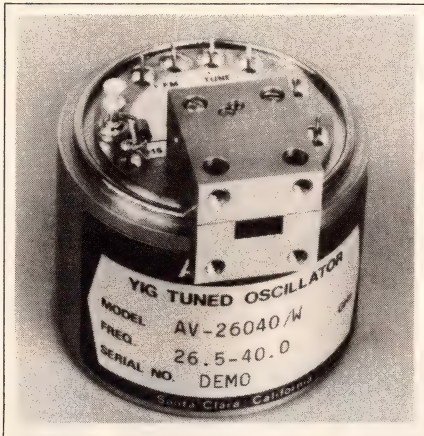


- 1) XVME 010 System Resource
- 2) XVME 085 VMEbus Prototyping
- 3) XVME 560 64/32 Channel Analog Input
- 4) XVME 220 32 Channel Isolated Digital Output
- 5) XVME 530 8 Channel Isolated Analog Output
- 6) XVME 240 64 Channel Digital TTL I/O
- 7) XVME 260 32 Channel Relay Output
- 8) XVME 080 Intelligent VMEbus Prototyping
- 9) XVME 210 32 Channel Isolated Digital Input
- 10) XVME 230 Intelligent Counter/Motion Control
- 11) XVME 420 Intelligent Serial Peripheral Controller

The Hardhat Computer People. 750 North Maple Road, Saline, Michigan 48176, Phone: (313) 429-4971, TWX 810-223-8153 **Regional Offices:** Boston (617) 246-2544 • Chicago (312) 963-7272 • Cleveland (216) 499-2555 • Houston (713) 530-9200 • Philadelphia (215) 536-0810 • San Francisco (415) 573-0404

CIRCLE NO 100

EDN June 13, 1985



OSCILLATOR

The AV-26040/W is a 26.5- to 40-GHz YIG-tuned, GaAs FET transistor oscillator with WR28 waveguide output. It features a minimum output power of 10 dBm with a maximum ± 3 -dB variation over the entire tuning range and a frequency-vs-tuning current linearity of $\pm 0.1\%$. The oscillator draws 150 mA from an unregulated 15V-dc supply. A 12-bit TTL-compatible driver or a 0 to 10V analog driver is optional. The unit combines a GaAs FET fundamental oscillator with two stages of single-ended GaAs FET amplification, followed by a balanced-amplifier output stage. \$3650. Delivery, 3 months ARO.

Avantek Inc., 3175 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-6710.

Circle No 376

TACHOMETER

The Tach-Pak 3 tachometer accepts magnetic speed sensor, sinewave, and TTL signals at frequencies from 0.0625 to 30,000 Hz and converts those signals to a meter output of 0 to 1 mA dc or an analog output of 0 to 20 or 4 to 20 mA dc. The unit also operates 5A spdt relays at four preset speed trip-points. Response time is 50 msec at frequencies above 100 Hz. The relay trip-points are field programmable via pushbutton switches. \$600.

Airpax Corp., Box 868, Cheshire, CT. Phone (305) 587-1100.

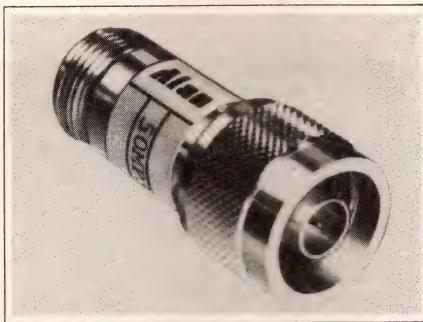
Circle No 377

SWITCHES

These wiping-contact and butt-contact pushbutton switches are available with a snap-in bezel that mounts from the front of a panel. The switches come in spst, spdt, and dpdt configurations, and they include such features as maintained action and overtravel. You can mate the switches with either a square or a rectangular bezel, which offers a choice of one or two snap-fit LED holes for applications requiring indicator lights. The square model inserts in a $\frac{3}{4}$ -in.² hole, and the rectangular model fits in a $\frac{3}{4} \times 1$ -in. hole. Six different colored button caps are available. \$2.51 to \$6.90 (100).

Grayhill Inc., 561 Hillgrove Ave, LaGrange, IL 60525. Phone (312) 354-1040.

Circle No 378



18-GHz ATTENUATOR

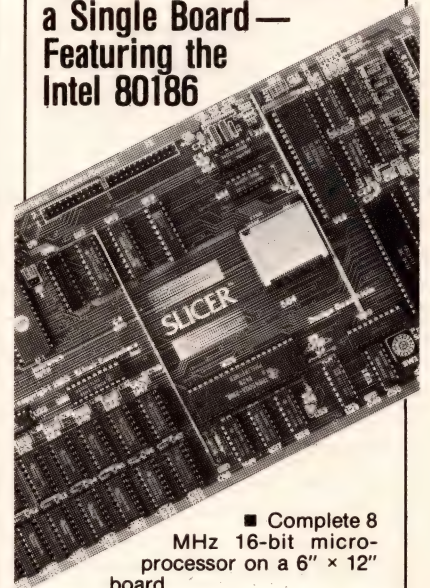
Model 50MP(1-40)-N is a fixed attenuator with a frequency range of dc to 18 GHz. It has an attenuation range of 1 to 40 dB in 1-dB steps. VSWR is 1.15:1 at dc to 4 GHz, 1.20:1 at 4 to 8 GHz, 1.25:1 at 8 to 12 GHz, and 1.35:1 at 12 to 18 GHz. The attenuator has a 50 Ω impedance and a type N connector per MIL-C-39012. Accuracy is rated at ± 0.3 dB from 1 to 6 dB, ± 0.5 dB from 7 to 20 dB, and ± 0.75 dB from 21 to 40 dB. Average power consumption is 2W and the operating range is -55 to $+125^\circ\text{C}$. From \$90.

Alan Industries Inc., Box 1203, Columbus, IN 47202. Phone (812) 372-8869.

Circle No 379

THE SLICER

Real 16 Bit Power on a Single Board—
Featuring the Intel 80186



■ Complete 8 MHz 16-bit micro-processor on a 6" x 12" board

- 256K RAM, plus up to 64K EPROM
- SASI port for hard disk controller
- Two full function RS232C serial ports with individually programmed transmission rates—50 to 38.4K baud
- Software compatibility with the 8086 and 8088
- 8K of EPROM contains drivers for peripherals, commands for hardware checkout and software testing
- Software supports most types and sizes of disk drives
- Source for monitor included on disk
- Bios supports Zebec 1410 and Western Digital WD 1002 SHD controller for hard disks
- Modifications available for specific applications

Fully assembled and tested only \$995. Also available in kit form.

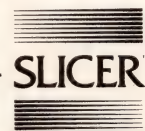
Operating systems are CP/M 86 by Digital Research, Inc. (\$85), and MS DOS by Microsoft Corporation (\$175).

Prices subject to change without notice.

Also available:

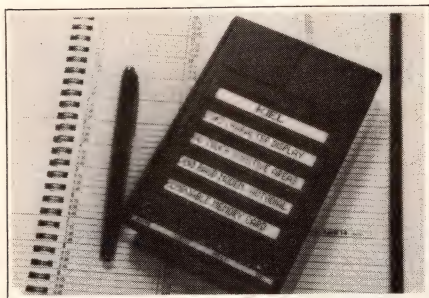
THE SLICER SYSTEM EXPANSION BOARD for expanded memory, additional ports, and real time clock.

The SLICER PC EXPANSION BOARD gives your Slicer high performance video capability.



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2543 Marshal St. N.E.
Minneapolis, MN 55418
612/788-9481
Telex: 501357 SLICER UD

COMPONENTS & PACKAGING



TOUCH TERMINAL

The Touch Pad I is a handheld touch-screen terminal capable of displaying 25 characters/line. Each line has 15 touch-sensitive areas. The terminal can display one to five lines of data and operates in an interactive mode with a host computer or smart terminal. An optional 48k bytes of RAM is available for off-line data acquisition. A memory program card, which is specific to the application, contains all the screens that you want to display. To change programs, you insert new memory program cards. You devel-

op the programs on a μ C with the manufacturer's program generator. The unit measures 6.3 $\times$ 4.1 $\times$ 0.8 in. <\$250 (OEM qty).

Kiel Corp., Box 6430, Nashua, NH 03063. Phone (603) 881-8666.

Circle No 380

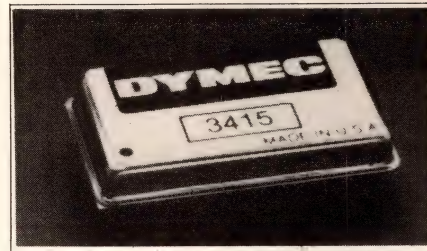
TOUCH SCREEN

The Microtouch screen offers touch resolution of 256 $\times$ 256 points. According to its manufacturer, the glass overlay sensor allows transmission of as much as 85% of the display's light. The sensor also conforms to the CRT surface, eliminating parallax problems. The controller transmits touch data over an RS-232C serial line to the host computer. It digitizes 50 points/sec in the stream mode or 1 point/touch in the point mode. You can program different data formats and store calibration values in onboard nonvolatile memory. The screen comes in 12-, 13-, and 19-in. sizes; custom

sizes are also available. You can purchase the Microtouch screen in kit form or already installed in the company's line of Point-1 monochrome or color monitors. 13-in. version, <\$500 (OEM qty).

Microtouch Systems Inc., 400 W Cummings Park, Woburn, MA 01801. Phone (617) 935-0080.

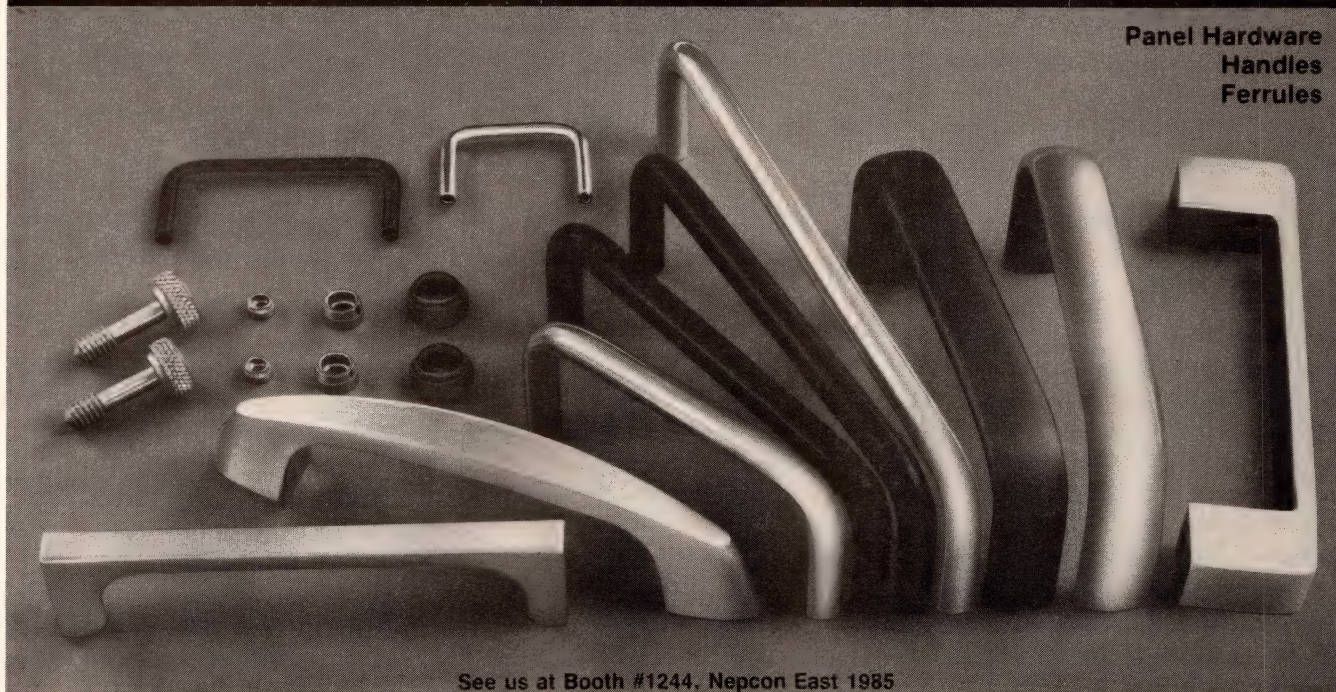
Circle No 381



S/H AMPLIFIER

Combining 200-nsec acquisition time with 150-nsec sample-to-hold settling time, the Model 3415 sample-and-hold amplifier offers $\pm 0.005\%$ FSR linearity. Offset is

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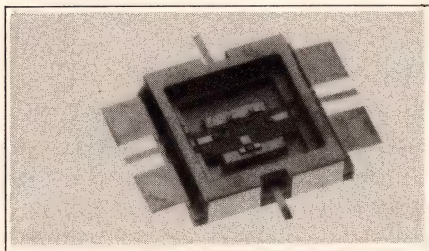
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COMPONENTS & PACKAGING

± 5 mV, with drift held to ± 50 $\mu\text{V}/^\circ\text{C}$ max. Other specifications include 1-mV pedestal, 90-dB min feedthrough, and 50-mA output at $\pm 10\text{V}$. The amplifier requires $\pm 15\text{V}$ typ and dissipates 720 mW typ, 875 mW max. Operating range is -25 to $+85^\circ\text{C}$. The unit comes in a 24-pin hermetic package and is a pin-compatible replacement for the SHC803CM. \$163 (100).

Dymec, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870.

Circle No 382



GAIN MODULES

The G-PAC gain and power modules are broadband gain-package amplifiers that perform over the 2- to 8-GHz frequency band and measure $0.52 \times 0.52 \times 0.11$ in. The 2-stage gain model offers a gain of 12 dB min and gain flatness of ± 0.75 dB max. It delivers 11-dBm output power at the 1-dB compression point. The power-block module specs a gain of 8.5 dB min and a gain flatness of ± 0.75 dB max. Power output is 19 dBm at the 1-dB compression point. Gain response changes less than ± 0.6 dB from -54 to $+85^\circ\text{C}$. Input and output VSWRs are less than 2:1; noise figure is less than 5.5 dB at 25°C . Both devices require an 8V supply. \$300.

Gould Inc, Microwave Products Div, 2580 Junction Ave, San Jose, CA 95134. Phone (408) 943-9055. TWX 910-338-0180.

Circle No 383

ATTENUATORS

Model 54 dc to 40-GHz fixed coaxial attenuator is available in values of 3, 6, 10, 20, 30, and 40 dB. SWR is

1.35 from dc to 26.5 GHz and 1.60 from 26.5 to 40 GHz for all units. The attenuator suits use in telecommunications systems, EW, radar, and other K and Ka band applications. Each attenuator is 1.75 in. long and measures 0.25 in. in diameter. The unit's 1W power rating (200W peak) over an operating range of -55 to $+125^\circ\text{C}$ is derated

linearly to 0.1W at 125°C . Each unit employs the manufacturer's WPM-4 connectors, which mate with SMA per MIL-C39012. \$295. Delivery, 90 days ARO.

Weinschel Engineering, 1 Weinschel Lane, Gaithersburg, MD 20877. Phone (800) 638-2048; in MD (301) 948-3434.

Circle No 384

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Arnold's unique line of miniaturized, high reliability power supplies lets you order tailor-made units from off-the-shelf sub-modules. Lead times are reduced to weeks and NRE charges are totally eliminated. Most importantly, you get performance and reliability that's been proven in thousands of demanding government/military applications.

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CIRCLE NO 103

NEW PRODUCTS: ICs & SEMICONDUCTORS

NEW SWITCHMODE III HIGH VOLTAGE TRANSISTORS IN TO-218

DEVICE	CURRENT RATING	$V_{CE(sat)}$	V_{CEV}
MJH16002-4	5	450	850
MJH16006-8	8	450	850
MJH16010-12	15	450	850
MJH16002A	5	500	1000
MJH16008A	8	500	1000
MJH16010A	15	500	1000
MJH16024-25	5	800	1500
MJH16028-30	8	800	1500
MJH16030	10	800	1500



1500V TRANSISTORS

The MJH16000 family of transistors for high-voltage switching and high-resolution CRT-deflection circuits includes units rated at 5, 8, and 15A, with V_{CEO} of 450 and V_{CEV} of 850V or V_{CEO} of 500 and V_{CEV} of 1000. Other units are rated at 5, 8, and 10A, with V_{CEO} of 800 and V_{CEV} of 1500. Inductive fall times range from 50 to 80 nsec, crossover times are from 70 to 120 nsec, and inductive storage times range from 500 to 800 nsec. The 450V models suit use in line-operated bridge and push-pull applications; the 500 or 800V versions suit line-operated, single-transistor flyback and converter applications. All devices come in TO-218 plastic packages. From \$1.58 (100). Delivery, stock to 12 wks ARO.

Motorola Semiconductor Products Inc., Box 20912, Phoenix, AZ 85036. Phone (602) 244-4912.

Circle No 385

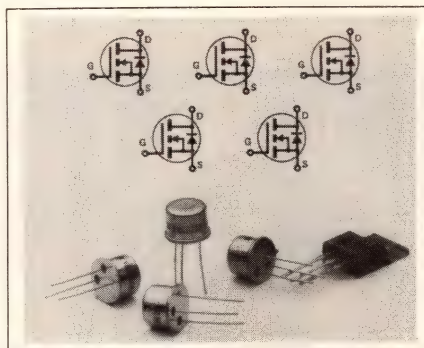
D FLIP-FLOP

The CD54/74HC273 and -HCT273 contain eight D flip-flops with common clear and clock lines. The HC versions suit use in high-speed CMOS-logic designs; the HCT models are speed, function, and pin compatible with LS TTL devices but dissipate less power than those units do. Propagation delay from the D input to the Q output is 13 nsec with the output driving a 15-pF capacitive load at 5V. Maximum clock frequency is 50 MHz typ. The -54-Series devices are supplied in 20-lead ceramic hermetic packages and operate over -55 to $+125^{\circ}\text{C}$. The -74-Series devices are housed in 20-lead plastic packages and operate

from -40 to $+85^{\circ}\text{C}$. The HC types run from supply voltages of 2 to 6V, while HCT types operate from 4.5 to 5.5V. 74HC/HCT273, \$1.70 (100).

RCA, Solid State Div, Rte 202, Somerville, NJ 08876. Phone (800) 526-2177.

INQUIRE DIRECT



MOS DEVICES

Suitable for applications that require low threshold voltage and compatibility with CMOS logic levels, VNC-, VND-, and VNE010 devices feature breakdown voltages of 60, 80, and 100V, respectively; turn-on threshold of 2V max; drain current of 4A; and on-resistance of 0.5Ω . All devices in the series feature a guaranteed threshold voltage of 3.6V max, high input impedances, low drive requirements, and a square safe-operating-area curve. They come in either TO-220 plastic or TO-39 packages. \$2.95 to \$4.02 (100).

Siliconix Inc., 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 387

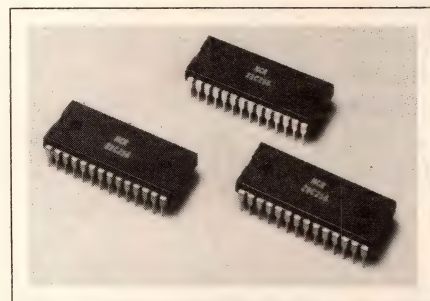
GRAPHICS IC

The enhanced 82720 graphics-display controller operates at 5 MHz and draws into a bit-map display at 800 nsec/pixel, a rate twice as fast as that of the company's original version of NEC's 7220 IC. The controller relieves the host μP of bit-map loading and refresh tasks. It also supports mixed graphics and alphanumeric displays; draws characters, points, lines, arcs, and rectangles; and permits zoom, pan, and

windowing via a 4M-pixel display memory. Less than \$40 (100).

Intel Corp., Literature Dept W-209, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-7602.

Circle No 388



256k-BIT CMOS ROM

The 23C256 CMOS static ROM, organized as $32\text{k} \times 8$ bits, features a 150-nsec access time. The device operates from one 5V power supply. In operating mode, current drain is 40 mA; in standby mode, the drain falls to 100 μA . A fully TTL-compatible device, the ROM suits use in portable and personal computers, telephone systems, robotics, and test equipment and comes in a 28-pin DIP with industry-standard JEDEC pinout. \$6.50 (10,000). Delivery, 6 wks ARO.

NCR, Microelectronics Div, 8181 Byers Rd, Miamisburg, OH 45342. Phone (800) 543-5618; in OH, (513) 866-7217.

Circle No 389

AUDIO D/A CONVERTER

The PCM53 Series of 16-bit monolithic audio D/A converters includes an internal zener reference, a resistor ladder network, high-speed current switches, and (on voltage-output models) a fast, low-noise op amp. The JP and KP models come in current (-I) or voltage (-V) output versions, and all provide 16-bit resolution, 96-dB dynamic range, and 16-bit monotonicity typ. Total bipolar drift and bipolar zero drift are ± 25 ppm/ $^{\circ}\text{C}$ of full-scale range (FSR) and ± 4 ppm/ $^{\circ}\text{C}$ of FSR, respectively. Typical settling time for



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ICs & SEMICONDUCTORS

the voltage-output units is 3 μ sec; the current-output models offer 350-nsec settling time. Operating temperature is -25 to $+85^{\circ}\text{C}$. The devices are compatible with industry specification EIAJ STC-007. JP-I and JP-V, \$17; KP-I and KP-V, \$19 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 390

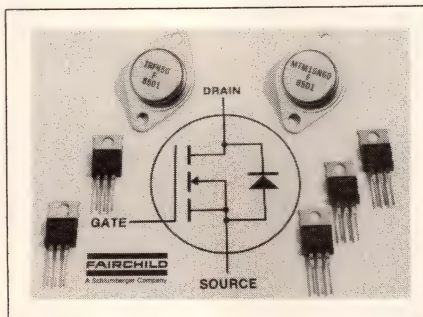
SPEAKERPHONE IC

The MC34018 incorporates the amplifier, attenuators, and control functions necessary to produce a speakerphone system. A peak-limiting AGC circuit inhibits speaker-amplifier clipping when the speaker is overdriven. The chip is powered by the phone line; onboard regulators provide voltage for the internal and external circuitry. A chip-select pin allows you to power down the

device. The circuit requires an external 2-to-4-wire converter and comes in a 28-pin DIP or a 28-pin surface-mount package. \$2.50 (10,000).

Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Phone (602) 897-8838.

Circle No 391



POWER MOSFETs

Implementing a proprietary design and manufacturing process, these six series of power MOSFETs spec ranges of 350 to 500V and 4.5 to

15A. Within this series, the IRF330-333 and MTM/MTP5N35 are 400 and 350V, 5.5A devices that dissipate 75W at 25°C and feature delay times of 30 and 55 nsec, respectively. Maximum on-resistance specs are 1 and 1.5Ω , respectively. The high-end IRF450-453 and MTM15N45 are 500 and 450V, 15A MOSFETs. Power dissipation at 25°C is 150W for the IRF450-453 and 250W for the MTM15N45, and respective turn on/off delay times are 35 and 150 nsec. Resistance specs are 0.4 and 0.5Ω max. The MOSFETs are available either in TO-220 plastic packages, with an operating range of -55 to $+150^{\circ}\text{C}$, or in TO-3 metal packages, for operation spanning -55 to $+175^{\circ}\text{C}$. \$2 to \$37.90 (100).

Fairchild Camera and Instrument Corp, Power Systems Div, 4300 Redwood Hwy, San Rafael, CA 94903. Phone (415) 499-4406.

Circle No 392



The **STM 4000** is a fully integrated digital function tester. Available at PC prices. **Perfect for incoming inspection** of digital ICs. Lets you automate inspection and reject bad ICs. Test MICROS, EPROMs, RAMs, ROMs, PALs, PLAs, PLDs, UARTs, 7400s, printed circuit boards, and custom/semicustom VLSI parts. Performs pass/fail tests, as well as detailed failure analysis.

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CIRCLE NO 106

MULTIPLEXER

The Si520 CMOS data-acquisition system combines an 8-channel multiplexer, a sample-and-hold function, an 8-bit A/D converter, and μ P control logic on one chip. The device offers conversion times as low as 70 μ sec plus a 14-kHz throughput rate. Linearity error equals ± 0.5 LSB max. Digital inputs and outputs have latchable 3-state buffering. The converter operates from one 5V supply and is housed in a plastic or ceramic 28-pin DIP, providing temperature ratings of -40 to $+85^{\circ}\text{C}$. \$7.50 to \$8.63 (100).

Siliconix Inc., 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

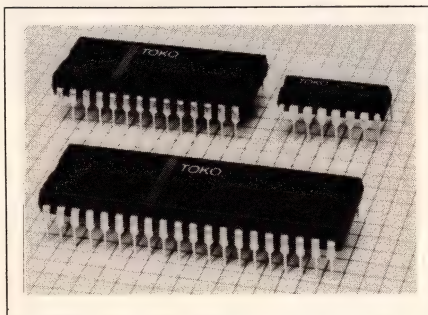
Circle No 393

SWITCHING DIODE

The PIN RF switching diode type DPJ 0350-034 operates with a resistance of 0.6Ω at a forward current of 3 mA. Typical capacitance is 1 pF at zero bias; it drops to 0.8 pF at 3V reverse bias. Minority-carrier lifetime is 50 nsec. The manufacturer guarantees a 35V reverse breakdown. The diode comes in an axial-lead DO-34 glass package; the company provides optional taped and reeled devices for quantities exceeding 10,000. \$0.36 (100).

SDI Inc., 11 Executive Park Dr, North Billerica, MA 01862. Phone (617) 667-7700.

Circle No 394



CONTROL ICs

Three CMOS LSI chips—the KM3701D function generator, KM3702D comparator, and

KM3703D feedback pulse generator—are now available in plastic packages. The -3701D generates interpolation pulses for two axes of movement, according to instructions from a host CPU. With the addition of the -3702D comparator, the -3701D can control dc servo motors. The -3703D monitors the direction of rotation of servo motors, as

sensed by an encoder, and transmits the information to the -3702D. A prototyping kit for 2-axis numerical control contains one -3701D, two -3702Ds, two -3703Ds, and documentation. \$155.

Toko America Inc., 5520 W Touhy Ave, Skokie, IL 60077. Phone (312) 677-3640. TLX 230724372.

Circle No 395

THE BEAUTY OF A ROGERS INTERFACE IS MORE THAN SKIN DEEP

We admit our MEKTRON® micromotion keyboard assemblies look good from the outside. We use a wide range of striking visual effects such as deadfronts, back-lighting and embossing.

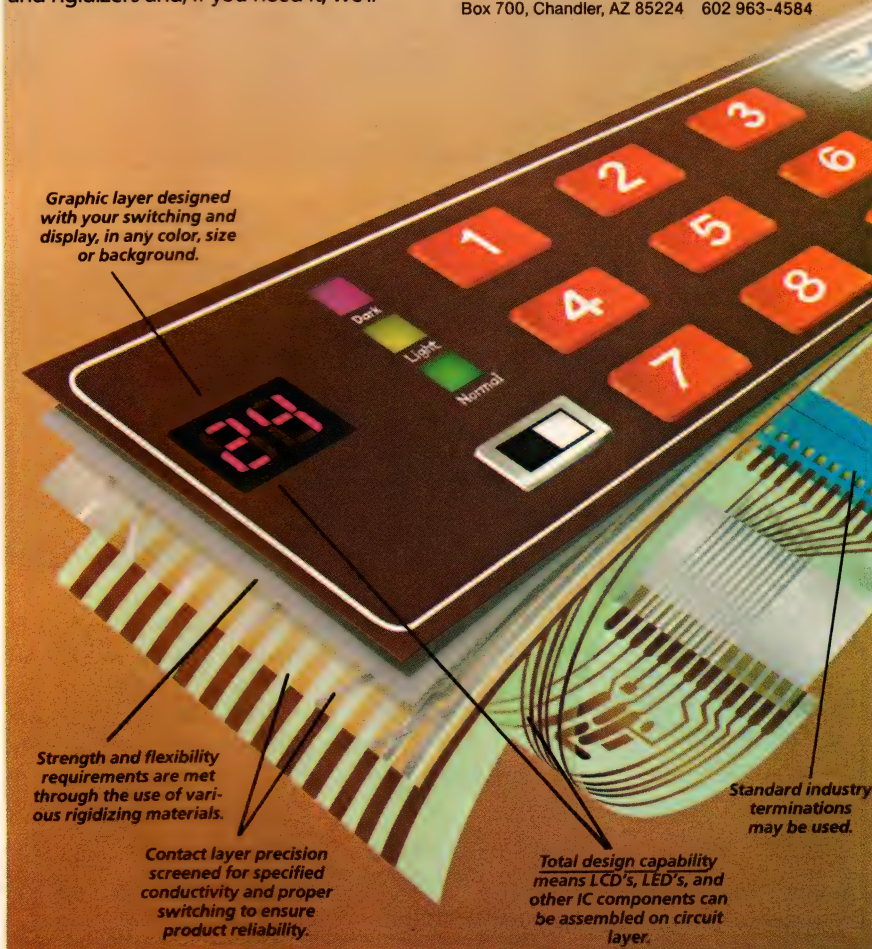
But the real beauty of our keyboards lies below the surface, in the total design capabilities we put behind them. Our engineering staff helps you choose the most economical and practical way of arranging switch functions. We select the proper dielectrics, conductors, adhesives and rigidizers and, if you need it, we'll

assemble your complete data entry system incorporating LED's, LCD's and IC's. We can even show you how a membrane keyboard assembly can be an easier, cost-effective alternative to full travel technology. We won't deny that it helps to have a pretty face in this business. But at Rogers, we think true beauty is reflected from the inside out.



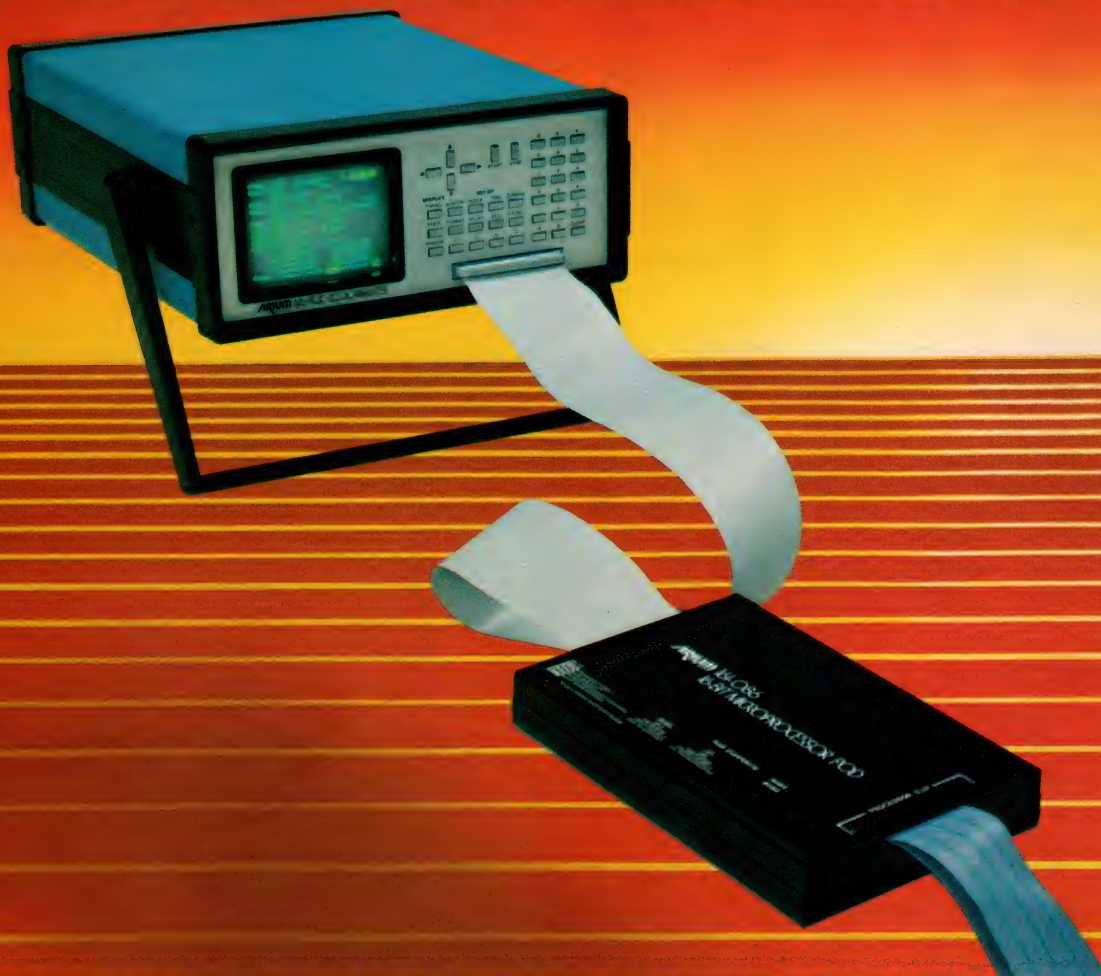
ROGERS

Rogers Corporation, Keyboard Division
Box 700, Chandler, AZ 85224 602 963-4584



CIRCLE NO 107

"Best performance in a 16-bit supporting role..." The Arium ML4100B Logic Analyzer.



At only \$2,675, Arium's full-featured ML4100B Logic Analyzer delivers more performance per dollar than any other logic analyzer:

- Disassembler support for Motorola 68000 and 68010, and Intel 8086 and 8088 microprocessors. (Optional)
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- FILTERED mode removes all non-executed prefetched cycles in the pod hardware.
- JUMP mode suppresses all but program control transfers and produces disassembled "map" of code location in actual execution.
- STATE display shows data as it occurs on address and data busses.
- DISASSEMBLY display shows reverse-assembled code mnemonics and labelled exceptions processing as they are actually executed by the processor (including data cycles **unscrambled** and put back

with their corresponding instructions).

```

STATE PC DISASSEMBLY 50000T S/U
-0010 000402 MOVE #2000,SR S
-0015 000406 NOP S
-0014 000408 MOVEA.L #00040400,A1 S
-0011 00040E MOVEA.L #00000200,A0 S
-0006 EXTERNAL INTERRUPT EXCEPTION
PC:0403FC<00000414 SR:0403FA<2000
VECTOR: 0001D8>05000500
TRIG 000500 MOVEA.L #00040200,A0 S
00003 000506 MOVEA.L #00040300,A1 S
00006 00050C RTE PC:0403FA>2000 S
00011 000414 ADD0.B #8,D0 S
00012 000416 ADD0.B #8,D1 S
f1=Pos, Cursor f2=Spd: slow f3=Cycles: on
    
```

- DISASSEMBLY display shows reverse-assembled code mnemonics and labelled exceptions processing as they are actually executed by the processor (including data cycles **unscrambled** and put back

```

STATE ADDR DISASSEMBLY X: 00B6T-0007
-0023 02B3B INT #10 S
-0020 SOFTWARE INTERRUPT TYPE 10 S
CS:00040>3FE0(IP) CS:00042>0000(CS)
SS:207FD<FC96(F) SS:207FB<0000(CS)
SS:207F9<2B3D(IP)
-0014 03FE0 IRET S
SS:207F9>2B3D(IP) SS:207FB>0000(CS)
SS:207FD>FC96(F)
-0004 02B3D STI S
-0003 02B3E NOP S
TRIG EXTERNAL INTERRUPT TYPE FF S
CS:003FC>3FE0(IP) CS:003FE>0000(CS)
SS:207FD<FE96(F) SS:207FB<0000(CS)
SS:207F9<2B3F(IP)
f1=Pos, Cursor f2=Spd: slow f3=Cycles: on
    
```

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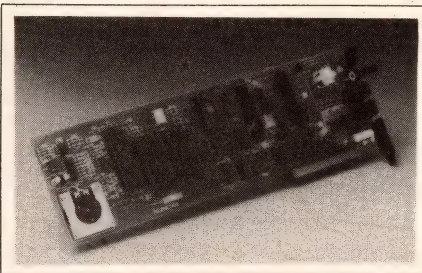
NEW PRODUCTS: COMPUTER-SYSTEM SUBASSEMBLIES

GRAPHICS CPU

By using two 16-bit CPUs, the Mega Machine lets you generate and animate 3-dimensional objects that won't show hidden surfaces. The real-time computer system operates with an IBM PC, PC/XT, PC/AT, or compatible computer, and the display system provides a 1024×768 pixel image area. You can display as many as 4096 colors on a color monitor screen simultaneously. Options include a digitizing frame buffer that captures and manipulates video images and a programmable audio synthesizer with six voices. The computer system contains an IEEE floating-point math processor, and the system's memory sizes range from 1M bytes to as much as 16M bytes. The manufacturer supplies Lumena graphics software and a diagnostic program with the system. From \$12,000.

Lazerus Productions, 2821 Ninth St., Berkeley, CA 94710. Phone (415) 845-1237.

Circle No 396



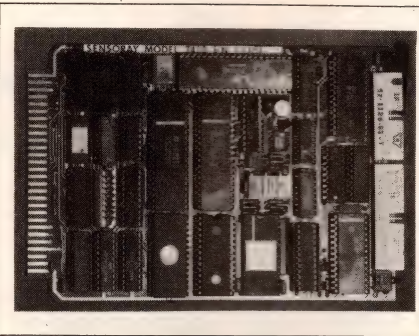
1200-BPS MODEM

The Expressdata 12i 1200-bps modem features adaptive equalization so that it adjusts automatically to varying telephone-line conditions. According to the company, this feature assures error-free and consistent performance over public telephone lines. The single-card modem plugs into the IBM PC and μ Cs having PC-compatible hardware. The asynchronous, full- or half-duplex device features autoanswer and autodial. The company's Relay software, which supports PC-to-PC and PC-to-mainframe communication, provides password and

encryption security and emulates 3270 terminals. The modem operates with most widely used communications packages. It meets Bell 212A and 103 standards and operates at 110/300 and 1200 baud. A call-monitoring feature detects busy, dial, and ringback signals automatically. \$495.

Telenetics Corp, 895 E Yorba Linda Blvd, Placentia, CA 92670. Phone (714) 524-5770.

Circle No 397

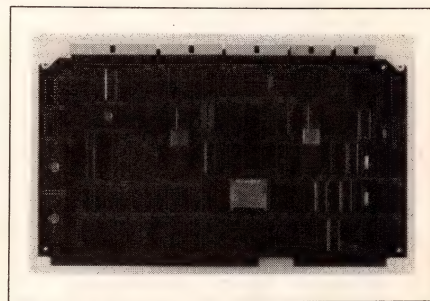


A/D CARD

The 7410 Series of STD Bus, data-acquisition processors suits use in process control, ATE, and laboratory systems. The interfaces combine a CMOS processor, a 12-bit A/D converter, serial and parallel communications ports, counter/timers, and 40k bytes of memory. Eight models are available; each comes with EPROM firmware for configuration as a dedicated interface. Thus you can construct multiprocessing and stand-alone systems from the basic 7410. The EPROMs provide a high-level command set that reduces software design time. The Z80-type code-compatible processors allow master/slave operation, DMA transfers, and vectored interrupts. STD Bus communication can also occur via two I/O ports. The 50- μ sec A/D converter includes a 16-channel multiplexer and sample/hold circuit. Multiple 7411T terminations can expand A/D channel capacity to 256. \$600.

Sensoray, 1445 Koll Circle, Bldg 112J, San Jose, CA 95112. Phone (408) 998-7271.

Circle No 398

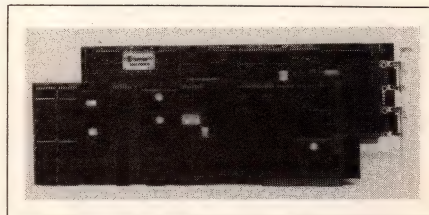


MULTIBUS BOARDS

The iSBC 214 and iSBC 226 multi-function single-board computers control peripheral storage devices in Multibus-based systems. The -214 provides standard interfaces to Winchester disk drives, floppy-disk drives, or streaming-tape drives. It controls as many as two 5¼-in. Winchester disk drives compatible with the ST506/412 standard, as many as four 5¼-in. floppy-disk drives (SA450/460 compatible), and as many as four ¼-in. streaming-tape drives (QIC-02 compatible). The board supports 20- or 24-bit addressing. The -226 board supports the enhanced version of the SMD interface. Intended for the control of high-performance, high-capacity hard disks, the board controls as many as two drives, compatible with the SMD interface, at rates to 1.9M bytes/sec. Both boards offer onboard diagnostics and error-correcting circuitry. The iSBC 214 and iSBC 266 cost \$1450 and \$2700, respectively.

Intel Corp, Literature Dept W-184, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (503) 640-7147.

Circle No 399



PC GRAPHICS

The M-16 and M-256 plug-in graphics controllers and the CD-1 RGB monitor are compatible with the IBM PC/XT, PC/AT, and the PC

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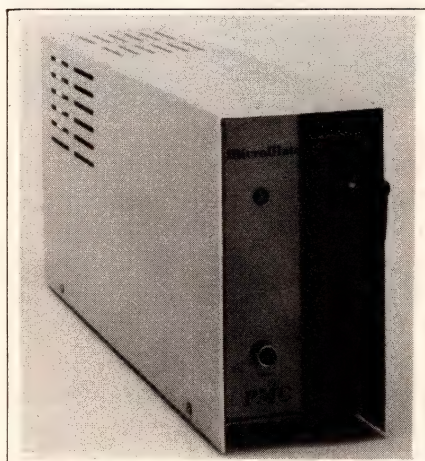
CIRCLE NO 109

COMPUTER-SYSTEM SUBASSEMBLIES

expansion board. The M-16 and M-256 controller cards can draw images at 1M pixels/sec and provide a choice of 16 and 256 colors, respectively, from palettes of 4096. They each have a 68000 CPU on board and a proprietary CMOS graphics controller chip. The CD-1 60-Hz, noninterlaced RGB display offers 640×480-pixel resolution. These three products are compatible with the IBM color-graphics adapter and support VDI and Halo graphics standards. Controllers, \$2250 to \$2850; display, \$1025.

Verticom Inc., 545 Weddell Dr, Sunnyvale, CA 94089. Phone (408) 747-1222.

Circle No 400



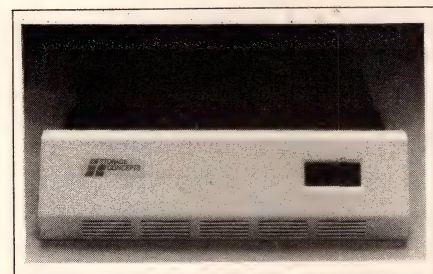
SINGLE-BOARD CPU

The Micromate computer is available as a single board for OEMs and systems integrators to incorporate in system designs. Designated Model PC-101, it has two serial ports, one parallel printer port, one floppy-disk interface for a maximum of four drives, and one high-speed parallel I/O bus with seven address lines for customized control interfaces. A 10M-byte hard-disk drive is available. The CPU interfaces to any standard ASCII terminal through one of its RS-232C serial ports. These ports are software programmable to independent baud rates from 50 to 19.2k. The OP/SYS software package option includes CP/M 3.0, PMC and CP/M utilities, and documentation. The Micro-

mate's BIOS source code, CP/M programmer's utilities, and bundled applications software is unbundled from the hardware for purchase as a package with the board, if desired. Model PC-101, \$495; software package, \$185.

Personal Micro Computers Inc., 275 Santa Ana Ct, Sunnyvale, CA 94086. Phone (408) 737-8441. TWX 910-379-5022.

Circle No 401



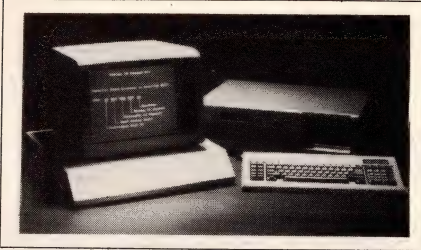
DISK SUBSYSTEM

Consisting of a controller and parallel transfer disk, the Concept 21 disk subsystem operates at transfer rates as fast as 9.3M bytes/sec to support real-time image-processing and communications applications. It's available with adapters for Multibus, Q Bus, Unibus, Versabus, and VME Bus computers. The disk subsystem can command five channels of disk I/O from one drive, with each channel operating at a 1.86M bytes/sec peak transfer rate. The controller uses a formatting scheme to maximize the peak transfer rate to 9.3M bytes/sec for the five channels with a storage capacity of 474M bytes on each of as many as four disks. The user provides the software to access the subsystem's command sets via a host adapter port. With the diagnostics command set, you can initialize the drive and controller at system start-up or when an error occurs. Using the maintenance command set, you can format the disk to account for bad sectors and bad cylinders before beginning a read or write operation. \$17,700.

Storage Concepts Inc., 3198-G Airport Loop Dr, Costa Mesa, CA 92626. Phone (714) 557-1862.

Circle No 402

COMPUTER-SYSTEM SUBASSEMBLIES



SINGLE-BOARD μ C

The Scadar Series 10 self-contained μ C system can be installed close to a process-measurement area, thus minimizing sensor and signal wiring. Analog-input modules interface directly to low-level sensors or high-level signals (from 4 to 20 mA and 1 to 5V dc). Two-wire transmitter power is included. All communications, I/O scans, and routine functions are controlled by the 16-bit 8088 CPU and internal firmware. Complete with memory, power supply, and I/O, the unit interfaces with IBM PCs and Intel 310/A and HP-3000 systems and DEC LSI-11, PDP-11, and VAX computers via

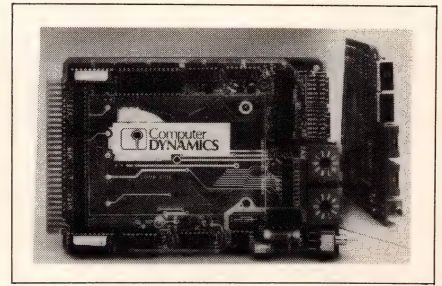
RS-232C and TTY current loop ports. ASCII characters are used as the command/response protocol to or from the Series 10. Available plug-in modules include an analog-input module and an analog I/O module—each accepts eight differential inputs over a ± 10 V dc range. Scadar Series 10, \$2500; I/O modules from \$475.

Burr-Brown Corp., Data Acquisition and Control Systems Div, Box 11400, Tucson, AZ 85734. Phone (602) 747-0711.

Circle No 403

STD BUS BOARD

The Combo is an STD Bus-compatible board that lets you choose any combination of these options: a battery-backed real-time clock/calendar that has a start/stop command for time adjustment and software interrupts; a 25W card-mounted power supply providing 5V at 4A



and ± 12 V at 0.2A; a power-fail interrupt with an adjustable brown-out level and missing-pulse detector for every half line cycle; 2k or 8k bytes of battery-backed RAM; and dual 7-segment LEDs and thumb-wheel switches for an operator interface. Substituting a parallel I/O for the operator interface, you get eight parallel latched outputs, eight parallel buffered inputs, and a strobe on a 34-pin header. From \$125.

Computer Dynamics Inc., 105 S Main St, Greer, SC 29651. Phone (803) 877-7471.

Circle No 404

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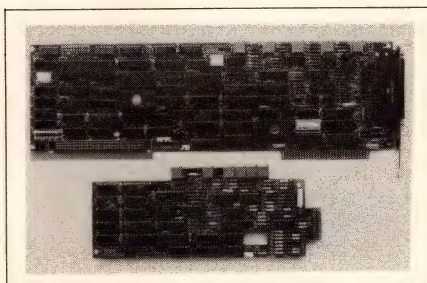


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COMPUTER-SYSTEM SUBASSEMBLIES



POWER CONTROLLER

The PPC100 interfaces an IBM PC to fixed-output power supplies and makes them programmable. Four isolated output channels allow you to configure as many as four programmable supplies in a system. Each output channel features 8-bit programming resolution and an optically isolated logic on/off control. An additional output for controlling ac system power with a solid-state relay is available. An onboard μ P allows you to create arbitrary waveforms to simulate ripple, noise, and voltage transients on the supply's outputs. An optional readback mod-

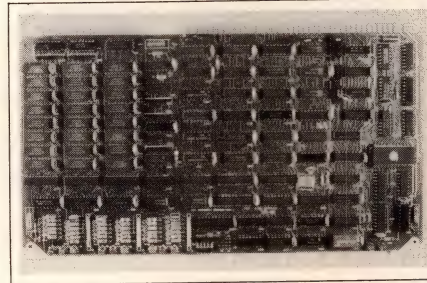
ule monitors voltage and current at each output and includes programmable overvoltage and overcurrent shutdown limits. An 8-bit A/D converter samples all eight readings every 160 μ sec. \$1260; readback option, \$590.

Carlton Industries Inc., 22661 Lambert St, Unit 207, El Toro, CA 92630. Phone (714) 770-7846.

Circle No 405

GRAPHICS BOARD

Multibus computer systems can use the RG-12C RGB color graphics board to display 512 $\times$ 240 pixels in any of eight colors on an RGB color monitor. The board provides both graphic and alphanumeric displays. Because the circuitry divides the onboard memory into four video display pages, you can store as many as four screen images at a time. The manufacturer claims that displays scroll smoothly. When you use the



board with a black-and-white monitor, you have a choice of eight shades of gray, or you can use three separate black-and-white display planes to drive three monitors. In addition, you can create one image from these three display planes. You control the board with a set of simple I/O commands. The board provides both a composite and a TTL video signal; it operates with either a 50- or 60-Hz synchronous frequency. \$695.

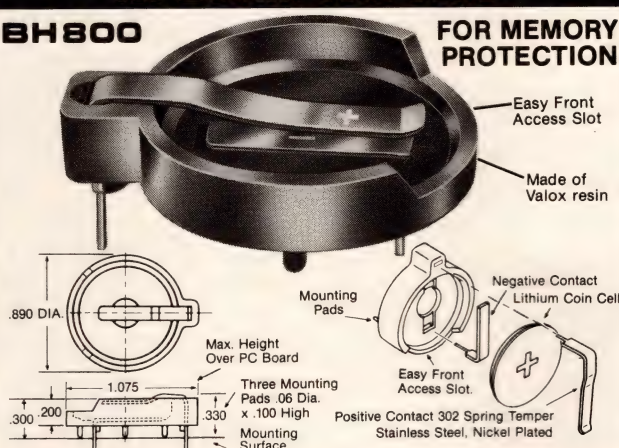
Raster Graphics Inc., Box 5157, Bend, OR 97708. Phone (503) 388-2584.

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Patent 4,487,820

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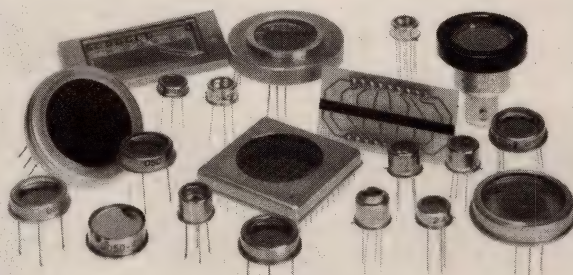
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THE COMPLIANCE REPORT—FCC/VDE/ESD

FCC special task force goes to work and seizes over 2,700 pieces of electronic equipment, mostly those regulated under Part 15 of its FCC Rules, in a sweep coordinated with the U.S. Customs Office. In addition to the equipment seizure, one man was arrested and arraigned before the U.S. Magistrate in the Eastern District Court of New York. If convicted, he will face up to five years of imprisonment.

A new special branch of the Commission announced that it had found a number of *cordless telephone* manufacturers to be out of compliance with Part 15, and sanctioned many in that industry, as well. (Part 15 prescribes mandatory emissions compliance for such devices as industrial and personal computers, peripherals, radios and televisions.) The newly organized branch dedicates its entire activities to spotting violators in the field and responding to complaints from competitors that others in their industry are not in compliance. According to sources close to the Commission, a special target will be those devices "verified" by the manufacturer as complying.

The East Coast's largest independent consulting firm, Dash, Straus & Goodhue, announced a new program to ease the chore of FCC compliance with either Part 15 or Part 68. Under the program, manufacturers can call in for a "guaranteed rate/guaranteed date" plan for having their equipment tested for compliance. And if the equipment does not comply, engineers at DS&G have a lengthy track record of quickly saving failing units with inexpensive fixes. DS&G's stamp of verification has been recognized by government authorities around the world.

If an application must be made with regulatory authorities, DS&G's in-house legal staff, which includes telecommunications attorneys, will prepare all the paperwork. Should the FCC call, DS&G will be there to give the Commission answers to any questions they may have concerning the product's compliance. The same program is now applicable to meeting the more stringent European mandatory EMI regulations.

VDE regulations reissued. Under West Germany's "Hfrg" Law, all devices which produce any radio noise between 10 KHz and 3000 GHz must have a permit to be sold in West Germany. Sanctions for failure to comply, which can be triggered by a competitor's complaint, include fines, seizures, recalls and injunctions. But under a new *revision of the law*, certain select, properly equipped U.S. test facilities can issue that permit. (Formerly, VDE engineers had to do the testing themselves for permits to be issued.) Facilities such as Dash, Straus & Goodhue, recognized by certain German-based authorities, have already begun issuing the rights to use the new general permits.

Said one Fortune 500 company executive, "This has eased the burden of selling in Europe tremendously." Compliance with West German law implies *de facto* compliance with the laws of most Western European nations.

Citizens' action group ask for sanctions against telephone interconnect makers. A Washington-based citizens' action group has filed with the Federal Trade Commission and the Federal Communications Commission against several cordless telephone, modem and telephone answering machine manufacturers, alleging they have falsely advertised their equipment as having FCC approvals which the devices did not have. The complaints are currently pending before the Commission.

Lamented one industry executive, "The regulations are so complicated; we intended to comply, but we have difficulty keeping track of all the changes." Complaints have also been filed with the State of California, which has separate regulations over telephone interconnect equipment.

An information clearing house has been set up by Dash, Straus & Goodhue to provide the information on VDE, FCC Part 15 and Part 68 rule changes. Persons needing information on the latest changes in these complicated regulations can contact the company at 617-263-2662.

Part 68 test workstations have never been previously available in the market, according to Compliance Design Incorporated of Boxborough, MA (617-264-4668). Rather, manufacturers and test houses have had to jury-rig the necessary facilities. Now, in one compact workstation, all the equipment is available from a single source. The workstation has been filed with the Federal Communications Commission and, according to the company, will soon be filed with Canada's Department of Communication, as well.

ANSI's open area test site committee continues its work, and according to sources close to the Committee, the group, which is setting standards for how EMI test sites would be constructed, is reaching a consensus position that will soon be voted on by ANSI. This influential document will feature the use of a "Standard Site Method," ideal curves for both broadband and dipole antennas, and a "Reference Antenna Method" based on the nearly lossless antenna known as the Roberts Antenna,™ developed by Willmar Roberts while he was Assistant Director of the FCC's lab in Laurel, Maryland. The Roberts Antenna is currently available from Compliance Design Incorporated of Boxborough, MA.

DASH, STRAUS & GOODHUE, INC.
593 Massachusetts Avenue
Boxborough, MA 01719
617-263-2662

For information on DASH, STRAUS & GOODHUE, INC.
circle number 85

For information on Compliance Design Incorporated
circle number 196

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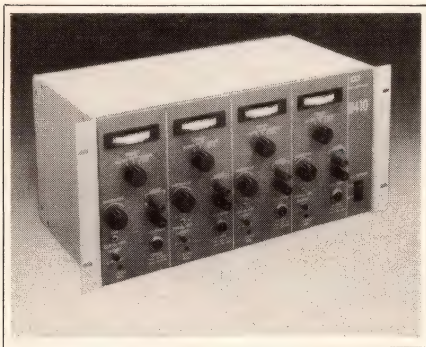


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LOAD MODULE

The D410 power-supply test instrument provides four individually programmable, isolated load channels with ratings as high as 50V at 10A. Each of the 0 to 10A, 2 to 50V loads can operate either manually or automatically with the manufacturer's test modules. In the manual mode, each channel has a constant-current range of 0 to 10A, $\pm 0.5\%$, and a slew rate of 1A/ μ sec. In the automatic mode, accuracy is $\pm 0.5\%$ with 12-bit resolution, stable to within 0.1% over a temperature range of 15 to 35°C. The 4-load cabinet is 16.5 in. wide, 8.75 in. high, and 10.375 in. deep. It weighs 15 lbs. \$2500.

Datapower Inc., Dept QTS, 3328 W First St, Santa Ana, CA 92703. Phone (714) 775-2000.

Circle No 407

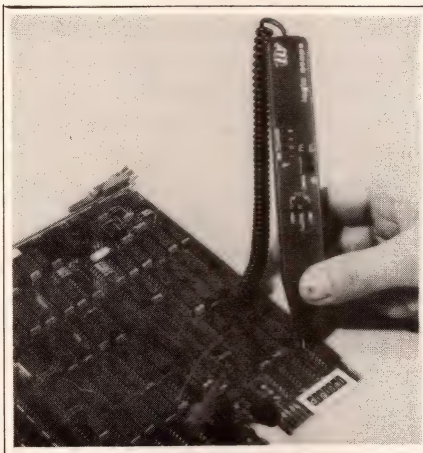
TEST SYSTEM

The PC1000 test and measurement system, which runs on an IBM PC, PC/XT, PC/AT, or bus, consists of as many as seven instruments in an expansion chassis. You can connect two chassis to the PC, thus yielding 14 instruments. The system features menu- or command-driven software. A semiautomatic mode allows you to run test sequences recalled from the PC's disk. The instrument modules include a 4½-digit autoranging multimeter, a 10- to 200-Hz low-distortion oscillator, a 0.01-Hz to 11-MHz function generator, a programmable 3-output power supply, a 125-MHz counter/timer, a 16-channel multiplexer pod, and an IEEE-488 interface.

Chassis \$1280, modules \$350 to \$950.

Vistar Corp., 13740 McCormick Dr, Tampa, FL 33624. Phone (800) 237-8812; in FL, (813) 855-6611. TLX 522434.

Circle No 408



LOGIC PROBE

The Logicscope handheld logic probe measures 10-nsec pulses at frequencies as fast as 45 MHz. Because the probe has eight LEDs with 3-color coding, it can indicate as many as 13 logic stages. For example, one LED clearly differentiates pulse trains from interference spikes. A binary counter with memory distinguishes between a pulse train and single pulses and indicates the results on four LEDs. Input capacitance is ≤ 2 pF, and the unit tolerates an overload of as much as 300V ac for five minutes. Test tips are replaceable. The company offers a 6-month warranty. \$85.

TEX Inc., Box 276, Martinsville, NJ 08836. Phone (201) 560-0588.

Circle No 409

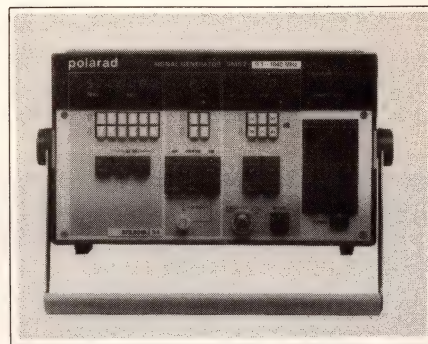
OSCILLOSCOPE

Model 9400 dual 125-MHz digital oscilloscope combines a 100M-sample/sec acquisition rate with 8-bit A/D converters and two 32k-word acquisition memories. It has an interleaved sampling rate of 12.5G samples/sec. You can control front-panel settings, display organization, and waveform processing with an

RS-232C port or an IEEE-488 interface. A 5×7-in. display shows internal status, measurement results, and software menus. A built-in plotter driver allows a hardcopy of the display. Capabilities include pretriggering and posttriggering, sequence and roll modes as well as standard triggering modes. The cursor allows you to measure voltage, time, and frequency of input and processed waveforms. You can store and recall as many as eight control settings manually or under external control. \$14,900.

LeCroy Research Systems Corp., 700 S Main St, Spring Valley, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

Circle No 410

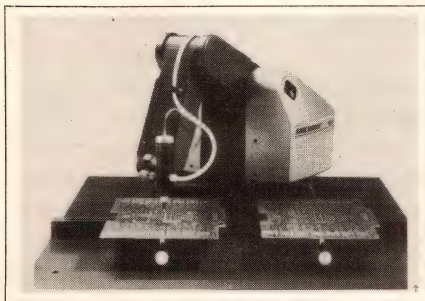


SIGNAL GENERATORS

Model SMS2 offers RF measurements within the range of 100 kHz to 520 MHz; option B2 extends the range to 1040 MHz. The generator has a 100-Hz frequency resolution. On AM/FM, the same features obtain a resolution of 0.05% (or 0.05 kHz). Spurious deviation is 3 Hz (CCITT weighting) or 15 Hz (30 Hz to 20 kHz). Phase noise is typically less than -125 dBc/Hz at a 20-kHz distance from the carrier and -145 dBc/Hz at 1 MHz. You can select channel-step sizes. Settling time is <40 msec. The built-in memory permits storage and recall of 40 settings for frequency, modulation, and output-signal level. \$7750.

Polarad Electronics Inc., 5 Delaware Dr, Lake Success, NY 11042. Phone (516) 328-1100.

Circle No 411



ROBOTIC DISPENSER

With the Alpha II robotic dispensing system, users can automate such electronic pc-board manufacturing tasks as solder masking and masking prior to conformal coating, as well as the dispensing of such materials as thermal grease, silicones, RTV, solder paste, adhesives, lubricants, and potting compounds. You program the robot arm with a joystick. The arm can move up and over components on stuffed boards and can tilt its needle to dispense material around the base of components. The robot also can

dispense materials onto large parts and assemblies that may require dispensing envelopes as large as 24×48×18 in. Featuring 5-axis movement, the robotic arm's controls include a mechanical gripper and two additional outputs for controlling conveyors, rotary index tables, or other devices that load, unload, or position materials or components on the board. The robotic arm without the computer system, \$21,825; complete dispensing system, \$24,950.

Microbot Inc., 453-H Ravendale Dr, Mountain View, CA 94043. Phone (415) 968-8911. TLX 4992310.

Circle No 412

MULTICOUNTER

The WD-757 universal counter measures frequencies, periods, totals, ratios, and time intervals. It furnishes ±0.003% accuracy and ±0.002% stability. The unit also fea-

tures three signal inputs and a switchable attenuator to reduce signals to 1/10 of their original value. A 10-MHz switchable lowpass filter passes or rejects signals below 10 MHz. \$479.

VIZ Test Equipment, 335 E Price St, Philadelphia, PA 19144. Phone (215) 844-2626. TWX 710-670-2626.

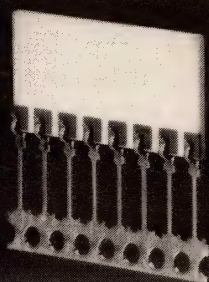
Circle No 413



PC POWER SUPPLY

Model HSC 130-40 is a 130W, 4-output power supply compatible with the IBM PC/XT. Typical ratings (fan-cooled) are 5V at 10A, 12V at 4.2A, -5V at 0.3A, and -12V at

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SAFT

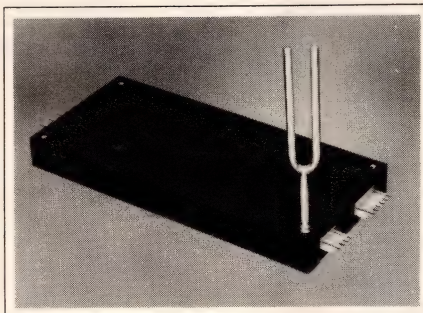
MORE POWER TO YOU.

CIRCLE NO 116

0.25A. Overload is set at 165W. The unit has two EMI line filters, is UL listed, and meets VDE 0806. Two ac receptacles are available for external peripherals. \$177.50.

Hughes Power Products Inc., 709 N Memorial Parkway, Station F, Huntsville, AL 35801. Phone (205) 534-0078.

Circle No 414



SMALL SWITCHER

The P100 Model, also identified as the Falcon, is one of a series of off-line switchers that incorporates a design that provides a power density of 5W/in³ within a 0.8-in.-high package. According to the manufacturer, this power density represents a threefold improvement over conventional open-frame supplies. The switcher is rated to 100W with outputs of 5, 12, -12, and -5V. Input is 110/220V. All heat-dissipating elements are thermally linked to a common baseplate to facilitate cooling by air flow, heat sinking, or normal convection. The device features 2% regulation, soft-start, autosequencing, short-circuit protection, and RFI filtering. \$126 (1000). Delivery, 10 to 12 wks ARO.

Theta-J Corp., 8 Corporate Pl, 107 Audubon Rd, Wakefield, MA 01880. Phone (617) 246-4000.

Circle No 415

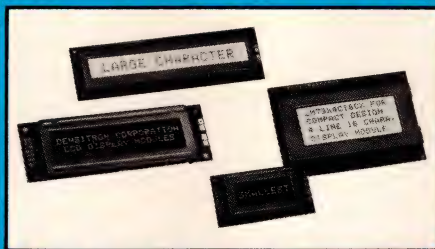
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1x16	5.73	2x40	12.71	64x240
1x16	7.95	2x80	3.31	64x320
1x16	12.71	3x40	3.52	64x480
1x20	3.80	4x16	4.15	128x128
1x20	12.71	4x20	5.55	128x256
1x24	5.50	4x20	12.71	128x480
1x24	12.71	4x40	4.85	200x640
1x40	5.50	4x40	12.71	
1x40	12.71	4x80	4.15	
1x80	3.31	8x20	3.66	
2x8	3.80	8x40	3.66	
2x16	4.55	8x80	3.45	
2x16	8.44	16x20	3.09	
2x20	4.85	16x40	3.31	
2x20	8.44	16x80	3.31	
2x20	12.71	25x80	3.10	
2x24	4.55	25x80	5.35	

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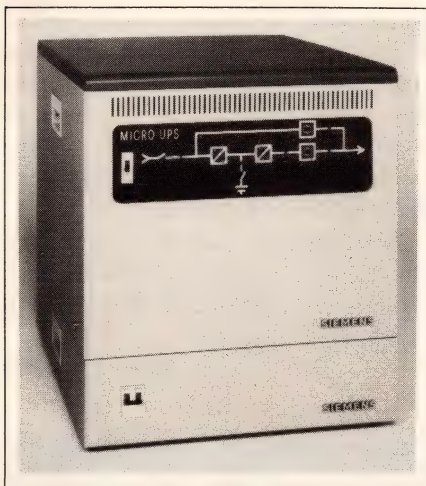
DATA-LINE MONITOR

The battery-powered, handheld Network Probe (Model 6620A) diagnoses problems in computer systems, data-communications networks, and peripherals. It incorporates the functions of a data-line monitor; a protocol analyzer; a programmable emulator; a bit/block error-rate tester; a digital meter that measures volts, ohms, and decibels; a speaker monitor; an RS-232C breakout status display; and a continuity tester. \$3495.

Network Communications Corp., 9600 W 76th St, Minneapolis, MN 55344. Phone (612) 944-8559.

Circle No 416

NEW PRODUCTS: INTERNATIONAL



UPSs

The Micro Series of uninterruptible power supplies includes units with power ratings of 0.5, 1.0, and 2.5 kVA. Controlled by a single on/off circuit breaker, the units feature automatic start-up and load connection after switch-on, and a mimic-diagram LED display to indicate the system status. A static bypass switch allows you to keep equipment on line while carrying out maintenance on the UPS. The units provide dc battery-charging current at 48V and therefore are compatible with standard telephone and telecommunications battery packs. Optional sealed lead-acid battery packs, which provide standby power for periods of 10 to 120 min, are available for mounting beneath the main unit. RF interference meets the requirements of BS800, and acoustic noise is below 50 dBA. From £1735.

Siemens Ltd, Windmill Rd, Sunbury-on-Thames, Middlesex TW16 7HS, UK. Phone (09327) 85691. TLX 8951091.

Circle No 417

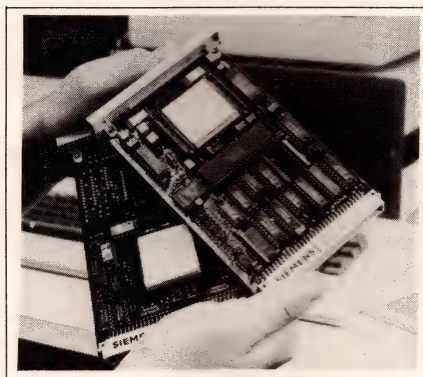
LINE FILTERS

The SUP-BR-E Series of pc-board-mountable line filters features current ratings of 2, 4, or 6A and meets UL, CSA, and VDE standards. RX732 filters, which are available in 1, 2, or 4A versions and have resin-sealed cases, also meet ASE re-

quirements. The filters operate over -25 to +85°C. Approximately £2.50 (1000). Delivery, 6 to 8 wks ARO.

Roxburgh Suppressors Ltd, Haywood Way, Ivyhouse Lane, Hastings, East Sussex TN35 4PL, UK. Phone (0424) 442160. TLX 957104.

Circle No 418



BUBBLE MEMORY

The PMS-S85B bubble-memory card for PMS μ C systems is expandable from 256k bytes to 1M byte of nonvolatile storage. Running under the CP/M-85 operating system, the memory is formatted to resemble a floppy disk. A 256k-byte version has 32 tracks, each with 64 sectors of 128 bytes/sector; expansion to 1M byte increases the number of tracks to 128. DM 8000.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 419

SPEECH PROCESSOR

Using the BA1701 variable-speech-control IC, you can maintain the intelligibility of recorded speech while replaying the recording as fast as 2.5 times the normal speed. Targeted at audio-cassette, dictation, and video-tape-recording equipment, the IC incorporates a PLL motor-speed controller to synchronize operation of the speech processor with the tape speed. The device also includes a unity-gain

buffer-amplifier, which typically introduces 0.2% THD. Supplied in a 14-pin DIP, the device operates from a 4 to 14V supply and requires 11-mA typ supply current. Approximately DM 10 (2000).

R-Ohm Electronics GmbH, Muhl-enstrasse 70, 4052 Korschenbroich 1, West Germany. Phone (02161) 61010. TLX 852330.

Circle No 420



DOT-MATRIX DISPLAY

Featuring 40 5-mm-high, 5×7-dot-matrix characters, the PVS35-05-40 vacuum-fluorescent display module has an onboard μ P to handle display multiplexing and interfacing. Its character generator produces a 96-character ASCII set, but you can download the module with 128 additional user-definable characters. You can program the display's brightness to one of eight levels; color filters can modify the color from blue/green to between orange/red and blue. The unit requires one 5V supply. Communication with the host system is via a serial or parallel TTL-level interface. £98.47 (100).

Pulseview Ltd, Unit 1 & 2, Suffolk Way, Drayton Rd, Abingdon, Oxfordshire OX14 5JY, UK. Phone (0235) 34909. TLX 83428.

Circle No 421

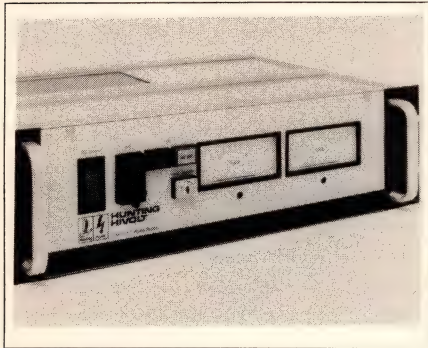
FORTH COMPUTER

The Forth Microcard runs with an RS-232C terminal and requires a development ROM for language development. In addition, this card has an autostart feature that lets you use it as the CPU in a computer system. The card runs an R65F12 μ P with an on-chip Forth kernel and includes two 28-pin, byte-wide

RAM/EPROM sockets. The processor's 40 I/O pins come on ribbon cable connectors. £119.

Essex Electronics Centre, University of Essex, Wivenhoe Park, Colchester CO4 3SQ, UK. Phone (0206) 865089. TLX 98440.

Circle No 422



POWER SUPPLIES

Utilizing switch-mode power-MOSFET techniques, the Series 250 high-voltage dc power supplies are able to deliver 250W. Various

models offer nominal outputs of 10, 16, 25, 30, 40, and 50 kV. They operate from a line input of 216 to 264V, 48 to 62 Hz, and have a line regulation ($\pm 10\%$ line change) of $\pm 0.02\%$ of nominal output. Zero to full-load output regulation is 0.05% of nominal output. The units are suitable for rack (19-in.) or bench mounting, and they operate over a range of 0 to 50°C, with an output TC of less than 200 ppm/°C. The supplies meet IEC348 Class 1 safety requirements and cost between \$1300 and \$2000.

Hunting Hivolt Ltd, Riverbank Works, Old Shoreham Rd, Shoreham-by-Sea, West Sussex BN4 5FL, UK. Phone (07917) 4511. TLX 87466.

Circle No 423

A/D CONVERTER

The SDA8010 IC performs an 8-bit A/D conversion in 10 nsec and dissi-

pates about 1W of power. Housed in a 24-pin ceramic DIP, the unit has a logic output that is ECL compatible. Applications include high-speed digitizing instrumentation, image processing, and medical systems. DM 994.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 424



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Type A-BP and A-BM solid state, pc-board-mountable relays switch ac loads of 3A rms (60A single-cycle peak) at voltages between 24 and



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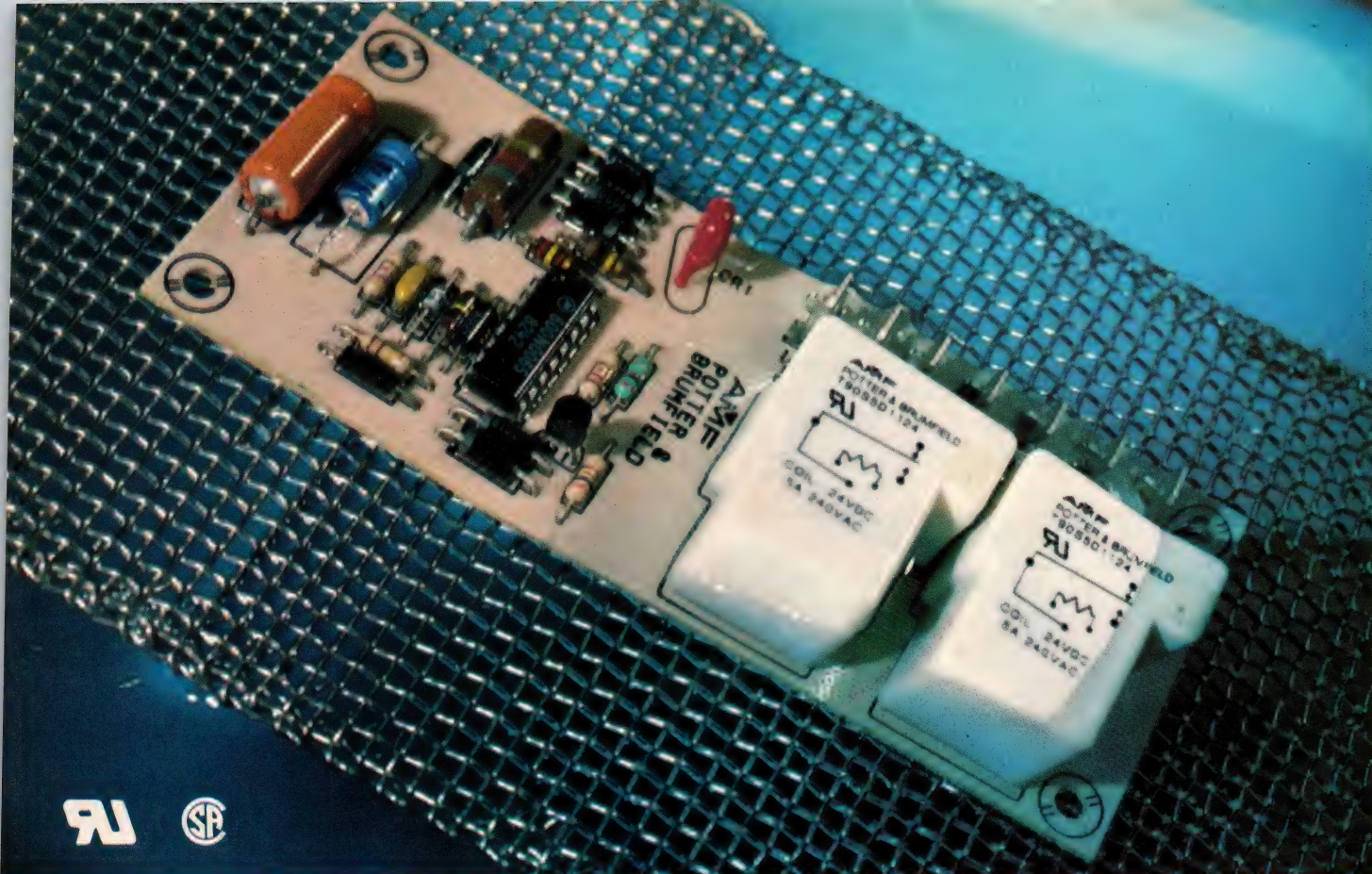
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EDN June 13, 1985



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Now you can design low cost power switching into your products with Potter & Brumfield's T90 relay.

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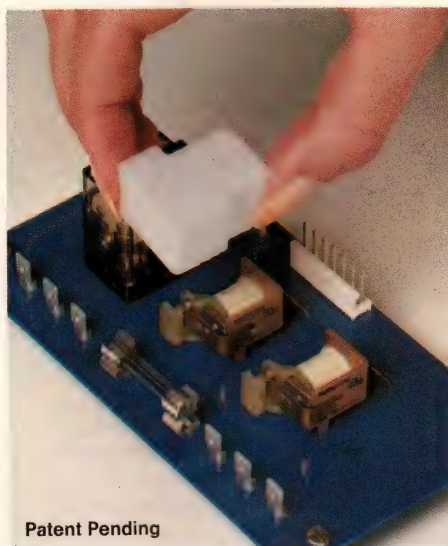
Its small size and low coil power requirement (less than 1W) make the T90 the ideal printed circuit board mounted interface between your solid state devices and power loads.

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CIRCLE NO 120

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Potter & Brumfield Division AMF Incorporated, 200 Richland Creek Drive, Princeton, Indiana 47671.

Regional Sales: Oak Brook, IL, 312/887-0811; Braintree, MA, 617/848-6550; San Juan Capistrano, CA 714/493-4503; Norcross, GA, 404/449-4601.

International Sales: Guelph, Ontario, 519/822-1576, TELEX: 0695-6522; Bristol, England, (0272)716301; Yokohama, Japan, (045) 812-1418; Hong Kong, TELEX: 39555; Singapore, TELEX: RS34686; Chatswood, N.S.W. Australia, (02) 411-5222.

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280V rms. They feature zero-voltage switching and require a minimum current of 5 mA to remain on. The devices have a maximum voltage of 1.6V rms when they are on and can withstand a minimum of 600V peak, with less than 1 mA of leakage current, when you switch them off. At switch off, their critical rate of change in voltage is 100V/

μsec. The relay's dc input control has a switching threshold between 1 and 3V and a switching delay of 10 msec maximum. The input is optically isolated with the output, which gives the relays 2.5 kV rms input/output isolation. The A-BP relay occupies 38×35.5 mm of board area and has an above-board height of 9.5 mm; type A-BM occupies 11×40 mm

of board area and specs an above-board height of 22.5 mm. Models for chassis mounting are also available with load current ratings of 10, 25, and 45A rms. A-BP, £3.45 (100); A-BM, £3.53 (100); versions for chassis mounting, £7.25 to £12.07 (100).

Allen-Bradley Electronics, Ennia House, High St, Edenbridge, Kent TN8 5LY, UK. Phone (0732) 866566. TLX 957293.

Circle No 425



How to meet your deadline and have your coffee too.

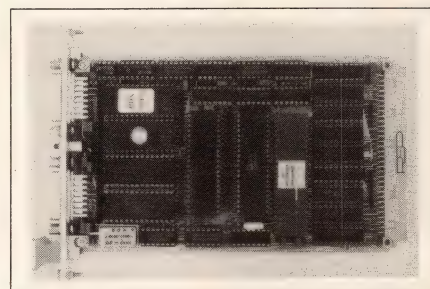
Find a converter, your boss says. Oh no you think, this could take hours or days with the design parameters he's specified. More precious time down the tubes. That's the way it is. *Unless* you have PARAMETRIX™ from INACOM International. Our Computer Aided Access helps you find integrated circuits by parameters in seconds. Frequently updated, PARAMETRIX provides a current source of comprehensive component information. And it's the only computerized parametric retrieval package that resides on your workstation. So you can concentrate on your real job ... *Designing*. And perhaps even have time to enjoy your coffee. To learn more about PARAMETRIX, the design time saver, call 1-800-443-INFO, 303/694-4200 (In Colorado) or drop us a line.

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CPU CARD

Containing a 68008 μP with speeds as fast as 16 MHz, the MPM68008 CPU card allows you to run 68000 code on 8-bit Euro-Bus systems or on the VME Bus. The board includes four 28-pin, byte-wide sockets. Three of the sockets accept either RAM or EPROM; the fourth one accepts only EPROM. The sockets accommodate devices with memories as large as 32k bytes. Using a PLA, you can program memory maps in the board's 1M-byte address range. The board also includes a 16-line parallel port with four control lines; two 16-bit programmable timers; and a serial I/O channel that you can configure for RS-232C, RS-422, HDLC, or SDLC protocols (any of which can be either asynchronous or synchronous) or for a fiber-optic link. \$330 (100).

PEP Elektronik Systeme GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 8974. TLX 541233.

Circle No 426

PEP Modular Computers Inc., 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661.

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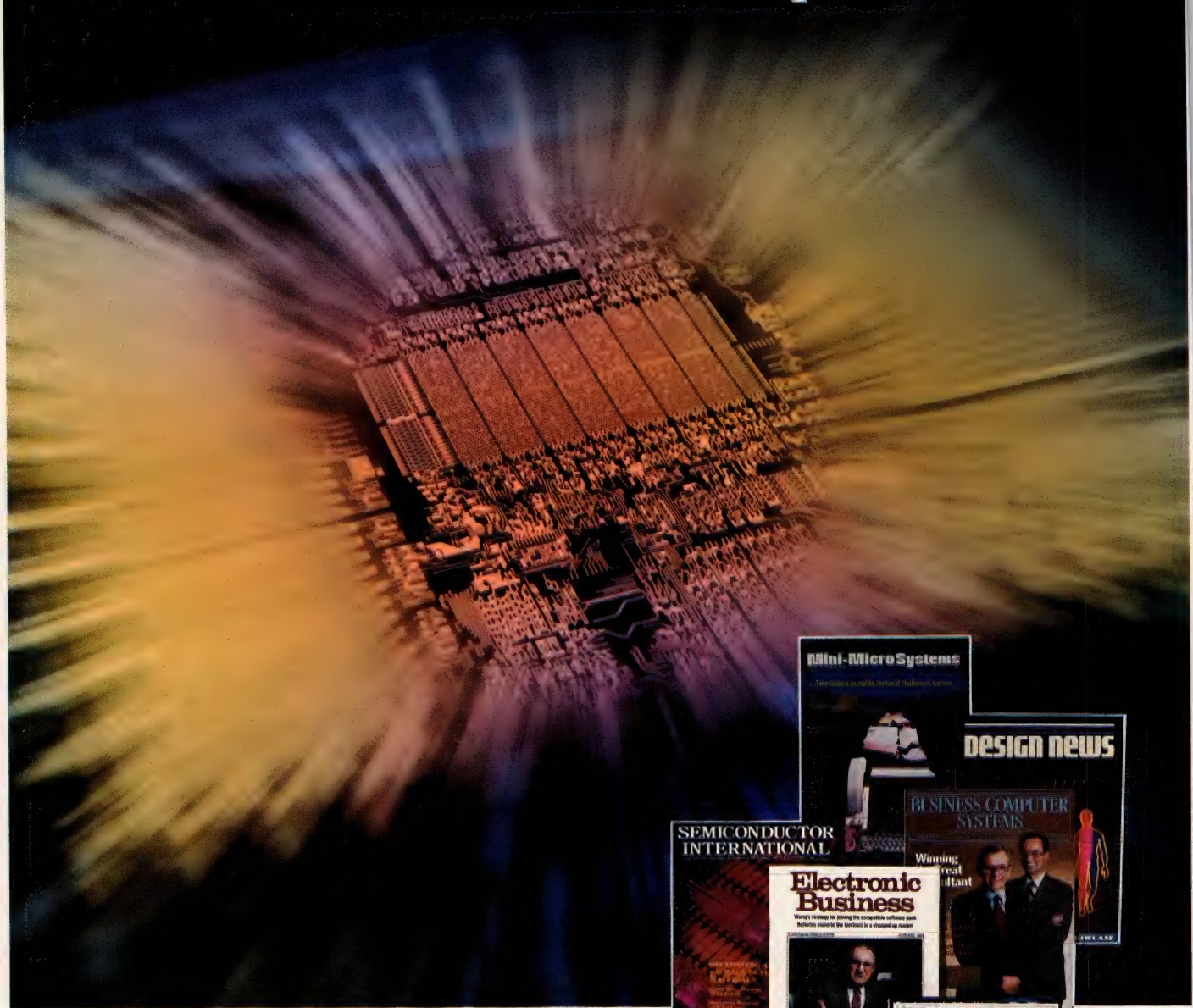
London (01) 837-2701, Paris (01) 531-7535, Milan (031) 67-9958, Munich (089) 59-4621, Seoul (02) 777-5767,
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NEW PRODUCTS: SOFTWARE

WORD PROCESSOR

A replacement for the copy-protected V 5.2, the unprotected Zardax V 6.0 permits user backup and program installation on most hard-disk drives running under DOS 3.3. The word processor features mail merge, a glossary of frequently used phrases, on-screen preview of printer output, printer spooling, and a cut-and-paste function. According to the company, its Utilities V 2.0 allows you to configure the program for use with various printer interface cards and with more than 50 different printers, including ink-jet and laser types. \$210; update for registered owners of Version 5.2, \$50.

Action-Research Northwest,
11442 Marine View Dr SW, Seattle,
WA 98146. Phone (206) 241-1645.

Circle No 427

PC/AT FORTH

Polyforth II, a multitasking, multi-user operating system, has been adapted for use on the IBM PC/AT. (This software-development system is available for the IBM PC and PC/XT as well.) Features include fixed-point fractional math, disk partitioning, kernel reconfiguring, tone generator control, inter-segment memory-access operations, and a graphics package for the standard IBM PC color adapter board. The graphics package features line drawing with texturing, color selection, vector math, vectored drawing functions, and aspect ratio selection. It also contains X-Y graphing routines and a documentation program. You can choose from several levels. Level 3 includes the operating system, Forth turnkey compiler, assembler, editor, math library, database-support system, utilities, graphics, and source code for everything but the nucleus. Level 4 includes all of the above features plus complete system source code and the company's Target compiler, which is capable of generating ROMable applications or recom-

piling the operating system itself. Level 3, \$600; Level 4, \$3200.

Forth Inc, 2309 Pacific Coast Hwy, Hermosa Beach, CA 90254. Phone (213) 372-8493.

Circle No 428



TERMINAL EMULATOR

Tektronix terminal emulation, VT100 terminal emulation, and four error-correcting, file-transfer protocols are combined in the VTERM/4010 package. On an IBM PC, PC/XT, PC/AT, or PC-compatible system, the emulator runs host software written for a Tektronix 4010, including Tell-a-graph, Sasgraph, and Plot-10. It also features printer and plotter support, throughput to 9600 baud, disk capture of graphics and text, support for Microsoft's mouse, setup screens, on-line help, and automatic dialing. The software emulates a 132-column display with horizontal scrolling. The file-transfer system includes Kermit; to use Kermit, you must obtain host software available from Columbia University. \$249.

Coefficient Systems Corp, 611 Broadway, New York, NY 10012. Phone (212) 777-6707.

Circle No 429

UNIX COPROCESSOR

The Opus516 personal mainframe is a Unix/coprocessor subsystem designed to transform an IBM PC into a 32-bit Unix workstation. The subsystem consists of a 32-bit coprocessor and a complete port of Unix System V (release 2.0) for the IBM PC and plug-compatible computers.

You negotiate transfers between Unix and DOS via a keyboard command. Based on an NS32016 CPU, the subsystem includes the 32082 MMU and 32081 floating-point unit. Onboard memory is expandable to 2M bytes. Included with Unix System V and its utilities are C and Fortran-77 compilers, an assembler, and a debugger. A 1M-byte configuration, including a single-user object-code license, costs \$3140 (OEM qty); multiuser licensing is available as an option.

Opus Systems, 960 San Antonio Rd, Suite 120, Los Altos, CA 94022. Phone (415) 941-7201.

Circle No 430

LIBRARIES

The 8096 FPAC/DPAC floating-point libraries are sets of subroutines used to process floating-point numbers in the proposed IEEE single- and double-precision formats. The libraries come in optimized source assembly language. The 8096 PFAC/DPAC library performs basic single-precision operations at approximately 12k floating-point operations/sec on an 8096 with a 12-MHz crystal. Double-precision operations run at about 5k floating-point operations/sec. The FPAC/DPAC 8096 library performs basic arithmetic, trigonometric, and exponentiation functions, and data-conversion and floating-point-utility procedures. Maximum code space for the single-precision routines is <3300 bytes; the combined single- and double-precision routines require 8100 bytes max of code space. Routines for double-precision basic operations comprise 1800 bytes, while single-precision operations constitute approximately 1M bytes of code. Single-precision 8096 FPAC, \$750; double-precision 8096 DPAC, including 8096 FPAC, \$1250.

United States Software Corp, 5470 NW Innisbrook Pl, Portland, OR 97229. Phone (503) 645-5043. TLX 4993875.

Circle No 431

ADA PROCESSOR

The GDADL processor is written in C and runs on VAX/VMS and VAX/Unix, Gould/UTX, and the HP-9000 Series 500 systems. With the processor, you can describe your concept of a design using structured English and still take advantage of the full set of Ada features. Specifying your system first in structured English lets you understand your design before you implement it in your target code. You can keep the design and the implementation-language source code in the same file for processing by both the source-language compiler and the Ada processor. By analyzing the structured English code and any Ada declarations you have made, the processor produces reports that reflect the design during any stage of development. The processor also generates a design description that highlights the control structures inherent in the design as well as any

module invocations and abnormal exits that are expressed in design code. \$7500; demonstration version, \$100.

Computer Systems Design, 3627 Padua Ave, Claremont, CA 91711. Phone (714) 625-6147.

Circle No 432

CP/M COMMUNICATIONS

Uniform, version 3.0, allows CP/M μ C users to read and write to data diskettes directly from different CP/M μ Cs. In addition, users can use it to initialize or reformat program or data diskettes for those machines. The program's enhancements include expanded user prompts and compatibility with more than 80 μ Cs—more than twice as many as permitted by the previous version. The utility permits transfer of files between CP/M and PC-DOS, MS-DOS, and many TRS-DOS files. It also allows easy file

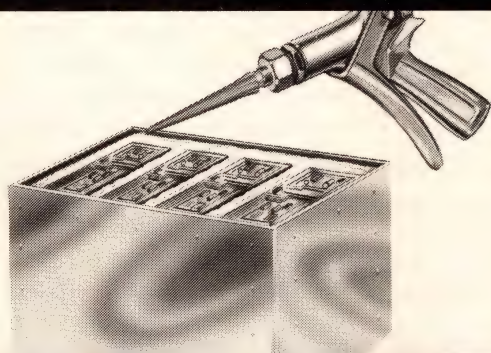
transfer of obsolete format CP/M diskettes to a format compatible with newer CP/M or MS-DOS machines. With the program, you can move any data file, including ASCII text, binary data, or program code, between CP/M and PC-DOS, MS-DOS, and compatible operating systems. \$69.95.

Micro Solutions Inc, 125 S Fourth St, DeKalb, IL 60115. Phone (815) 756-3411.

Circle No 433

REAL-TIME SOFTWARE

RTime is a software package for the company's Lambda family of Lisp machines that enables almost any Lisp program or expert system to perform real-time tasks, such as distributed process control. By implementing this program, the MC68010 coprocessor of the Lisp-based computer monitors and screens incoming information in real time. The



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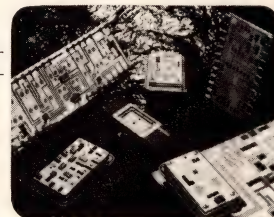
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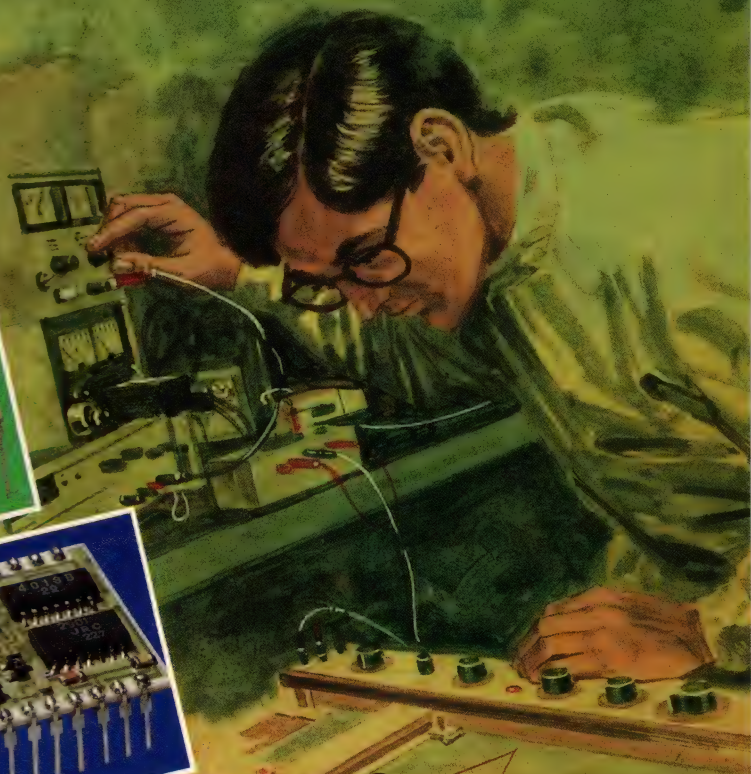
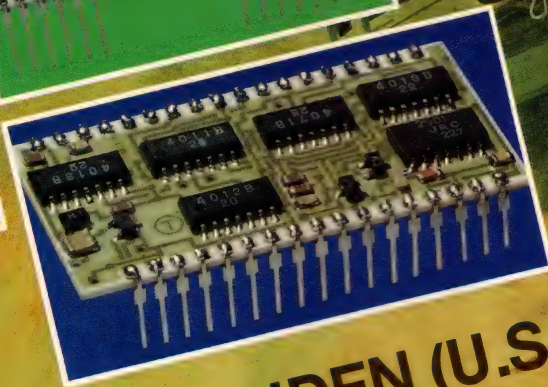
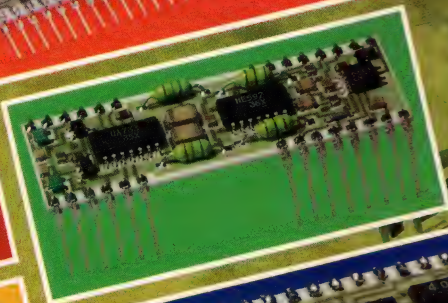
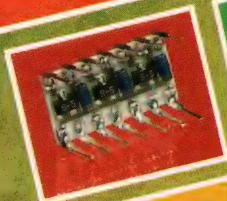
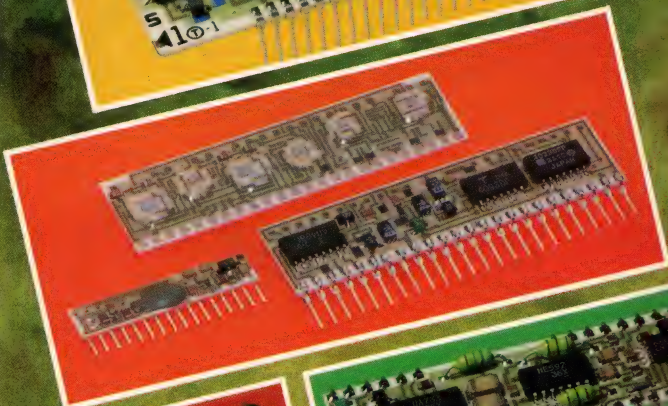
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CIRCLE NO 124

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package is written in C code. It operates in parallel with the Lisp processor and communicates with it via Streams (a Lisp-based serial interface) or by maintaining data values in arrays within shared memory. The software handles data acquisition, calculations, process-related algorithms, and low-level inferences or alerts. The Lisp processor can dynamically program this software either to monitor expected events or to focus on special areas of the process. \$20,000/license.

Lisp Machine Inc., 6033 W Century Blvd, Los Angeles, CA 90045. Phone (213) 642-1116. TLX 664608.

Circle No 434

VOICE MAIL

Soundtools allows developers to write voice-communications applications for an IBM PC. The package consists of a voice-communications card that fits in a half slot of an IBM

PC or PC compatible and a software program with documentation that includes the programming codes for developing applications. The following function calls are available: record a file, play a file, receive a Touchtone digit, and generate a Touchtone digit. The functions include fast forward, reverse, Touchtone abort, keyboard abort, and silence deletion. You can use the program with several languages, including C, assembly, and MS Basic A and Pascal. The software requires PC-DOS/MS-DOS 2.0, 2.1, or later versions. Speech sampling rate is 7 kHz; a compression ratio of 2:1 is achieved through the use of adaptive delta-pulse-code modulation. This ratio allows for approximately 1 hr of voice recording on a 10M-byte disk. \$449.

Digital Pathways Inc., 1060 E Meadow Circle, Palo Alto, CA 94303. Phone (415) 493-5544.

Circle No 435

SCREEN MANAGEMENT

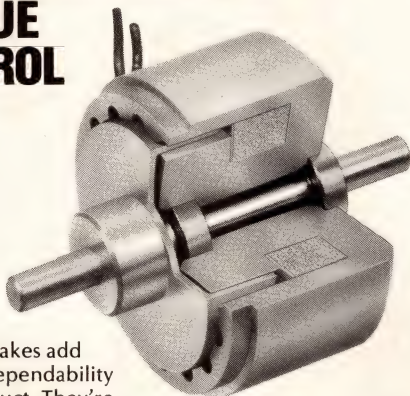
The XMenu/E information-display-management facility uses Rexx/Exec2 and other programming languages to create and display full-screen menus on display terminals. It supports all of the features of the 3270 family, as well as the 3180 and 3290, for creating menus as large as 256 rows×256 columns. Program function keys define 3270 fields with full control of attributes, including color and extended highlighting. You can assign alphanumeric names to fields for referencing by program. A Rexx/Exec interface allows run-time attribute changes, cursor positioning, and field-validity checking. \$1000, initial license fee and source code; \$2000, annual license fee thereafter with updated source code.

Kolinar Corp., 3064 Scott Blvd, Santa Clara, CA 95054. Phone (408) 980-9411. TLX 4998530.

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DID YOU KNOW

In February 1985, EDN sponsored the first Automated Design and Engineering for Electronics Conference and Exposition; the second ADEE conference will be in Boston in October.

EDN



Heat sinks, accessories inventoried

This updated catalog contains 92 pages on the manufacturer's heat sinks and related accessories. Text, graphs, and dimensional drawings present information on stamped, extruded, clip-on, and slide-on heat sinks. New products described include a low-cost heat sink that provides bidirectional cooling for LCCs, a clip-on heat sink for 12-pin SIPs, and slide-on heat sinks for 8-pin DIPs. Five pages of the 3-hole-punched catalog are devoted to new extruded heat sinks. Request *Catalog 1100*.

Aavid Engineering Inc., Box 400, Laconia, NH 03247.

Circle No 437

Interfacing a terminal with MIL-STD-1553 network

A 6-pg application note, *Designing a Remote Terminal to Talk with a MIL-STD-1553 Network*, discusses the interface that the BUS-65112 Superhybrid remote terminal provides to link a 1553B bus and the user's subsystem. The subsystem's interface comprises a 3-state, 16-bit parallel data bus, 12 address lines, DMA control lines, and status inputs and outputs. The brochure describes the remote terminal's design in detail as well as its built-in test and external clocking features. In

addition, the subsystem interface, error flags, and illegalizing mode codes are presented. Four figures and a table illustrate major points. A separate box defines the five functional blocks that constitute an MIL-STD-1553 LAN. Finally, five of the company's 1553 data bus products are illustrated and described.

ILC Data Device Corp., Marketing Dept, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 438



Primer explains UPSs

This 4-color brochure, designated Bulletin U-01302-3, explains how an uninterruptible power system can provide protection for a computer installation. It also describes the features for multimodule and single-module installations based on 350- and 426-kVA building blocks. The 12-pg primer details the firm's megawatt range of uninterruptible power systems, including descriptions of computer/overload fault protection, brownout protection, diagnostics, and space and cooling requirements. Figures and photos supplement the text.

Cyberex Inc., 7171 Industrial Park Blvd, Mentor, OH 44060.

Circle No 439

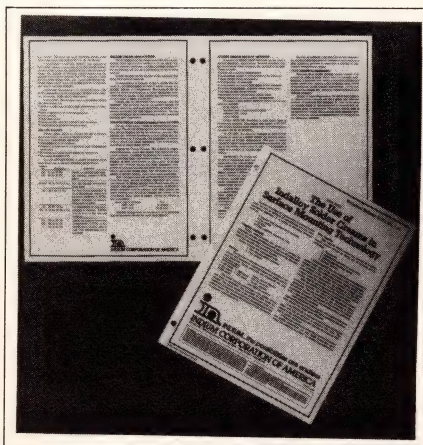
Compilation of switching regulator ICs

This data book contains 75 pages of summary technical information on the vendor's switching-regulator-IC products. Each entry includes prod-

uct features, applications information, absolute maximum ratings, system descriptions, and ordering information. In addition, the catalog reviews the fundamentals of pulse-width-modulated regulator circuits and presents several design and applications articles.

Exar Corp., Box 375, Sunnyvale, CA 94088.

Circle No 440



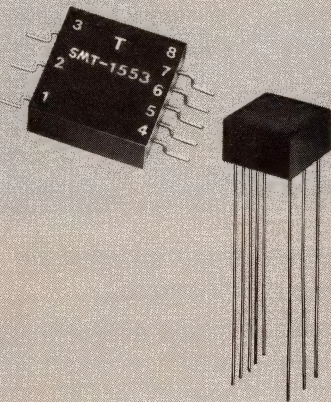
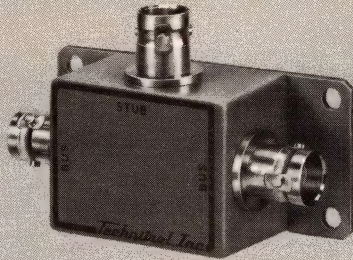
Learn use of solder creams for surface mounting

This technical bulletin details the use of the company's solder creams as a method of assembling electronic circuits with increasing densities. The data sheet describes how solder creams are formulated, what applications require which type of flux vehicle, characteristics of the available alloy compositions, and how the creams can be applied (screen printing, stenciling, or syringe). It also explains the curing process, which reduces spattering or solder balling, reflow methods, and flux removal. The bulletin suggests alloy combinations to satisfy surface-mounting applications found in printed flexible circuits and thick-film hybrid circuits. Other topics discussed include attaching chip components to the bottoms of pc boards prior to wave soldering and the use of alloys that help compensate for high TCE differences.

Indium Corp., Box 269, Utica, NY 13503.

Circle No 441

Mil-Std 1553 data bus couplers, interface transformers, absolutely to spec.



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Investigate our prices and large selection, including flat-pack and surface-mount 1553 interface transformers.

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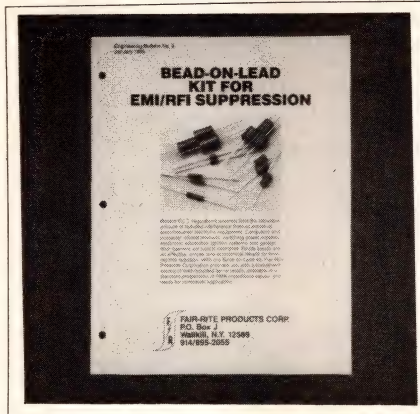
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CIRCLE NO 128

LITERATURE

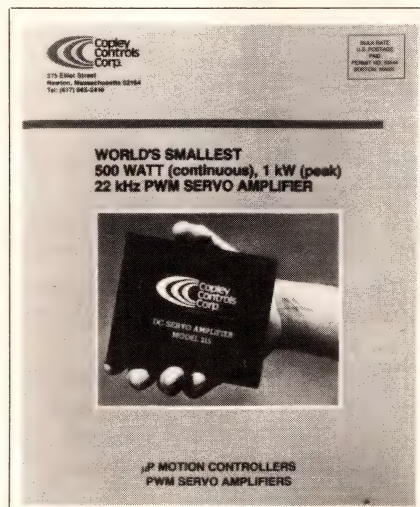


Use ferrites to solve EMI/RFI

This 4-pg data sheet (designated *Engineering Bulletin No 9*) describes a solution for reducing EMI/RFI through the use of ferrite components. The brochure begins with an explanation of the source of interference, continues with a discussion of the useful properties of ferrites, and concludes with a description of the manufacturer's bead-on-lead kit. Impedance values and physical dimensions for the beads in the kit are included. Seven figures supplement the text.

Fair-Rite Products Corp., Box J, Wallkill, NY 12589.

Circle No 442



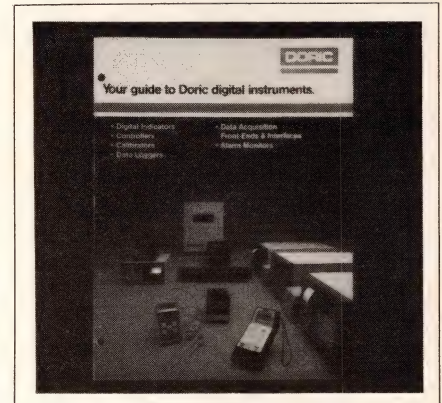
Specs for servo amps, digital controllers

This 2-color brochure details the manufacturer's line of servo amplifiers and digital controllers. Electrical and mechanical specifications are

presented for the 450 Series, which is an STD Bus-compatible servo I/O subsystem; Models 220 and 230, which are high-power, pulse-width modulation (PWM) dc amplifiers; and a small, modular series of PWM servo amplifiers. The catalog also presents product features, functional diagrams, drawings of outline dimensions, and ordering guides.

Copley Controls Corp., 375 Elliot St, Newton, MA 02164.

Circle No 443



Catalog depicts digital instruments

This catalog covers the manufacturer's line of digital indicators, controllers, calibration instruments, data loggers, data-acquisition front ends and interfaces, and alarm monitors. Specification tables provide information on input types, packaging, power requirements, and measurement ranges. The 20-pg brochure also highlights product applications. It comes 3-hole punched for loose-leaf filing.

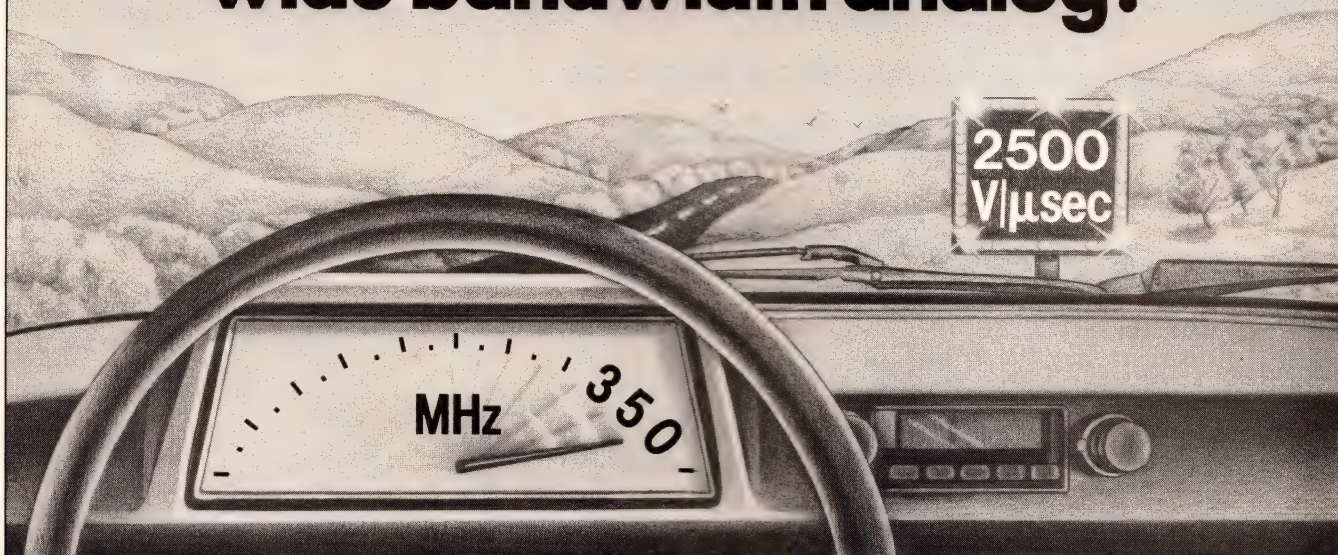
Doric Scientific Div., Rosemount Inc, 3883 Ruffin Rd, San Diego, CA 92123.

Circle No 444

Bibliography targets computer books

The 18th *Annual Bibliography of Computer-Oriented Books* lists more than 300 new publications. Although all introductory-type books published prior to 1982 have been deleted, the bibliography still contains over 1250 books from 155 pub-

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Device	Bandwidth	Slew Rate
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HOS-100	125 MHz	1500 V/μsec
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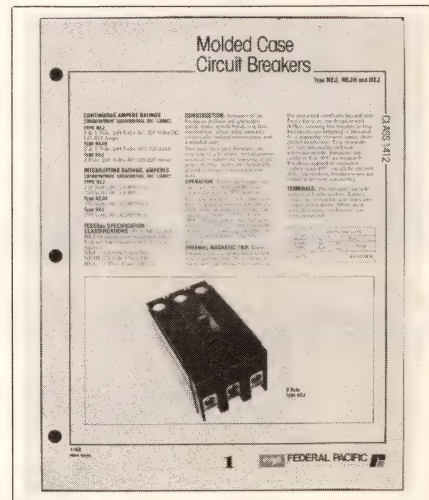
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Data sheet depicts circuit breakers

This 4-pg data sheet describes the manufacturer's NEJ, NEJH, and HEJ molded-case circuit breakers. The brochure details the circuit breakers' constructions, thermal magnetic trip, and terminals and how they operate. In addition, available accessories and modifications for the products are included. Dimensional drawings, selection charts, and time-current curves supplement the text. The data sheet is 3-hole punched.

Federal Pacific Electric, Marketing Information Center, Box 99457, Cleveland, OH 44199.

Circle No 445

Tome tabulates data on CMOS logic families

This 408-pg manual examines the company's ZX54/74AHCT advanced high-speed CMOS logic and ZX54/74HCTLS high-speed CMOS logic families. In addition to 120 data sheets, the compendium con-

LITERATURE

tains information on parameter measurements, enhancement programs, reliability, ordering information, and package dimensions. The book is free from authorized sales representatives, but costs \$5 if you order it directly from the company.

Zytrex Corp., 750 E Arques Ave, Sunnyvale, CA 94086.

INQUIRE DIRECT



Manual describes high-speed wire-wrapping

This manual, designated No S-3368, presents information on discrete wiring of high-speed logic. The book contains the Unilayer II test report, data sheet reprints of the company's ECL design panels, a flyer on Futurenet, a designer's guide, and a profile of the company's Interconnection Systems Division.

Augat Inc., Literature Dept, 40 Perry Ave, Attleboro, MA 02703.

Circle No 446

Bulletin covers solid-state timers

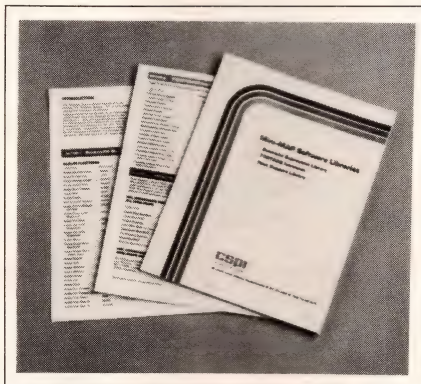
"Bulletin MM/MR-1" contains technical specifications, installation techniques, and application suggestions on two of the manufacturer's solid-state timers, which are designed to reduce setup costs and inventory requirements. The 6-pg brochure covers the SSF and SCF Series of multimode, multirange



timers. Charts, tables, and diagrams supplement the text. The bulletin is 3-hole punched for loose-leaf filing.

Amerace Corp., Newburgh Rd, Hackettstown, NJ 07840.

Circle No 447



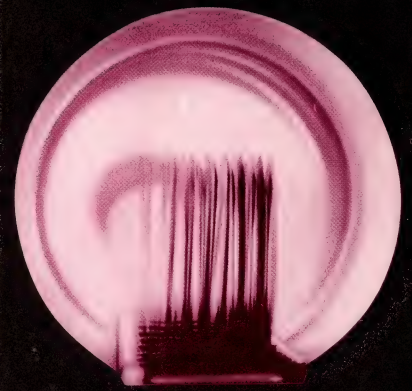
Array-processor software routines compiled

This 8-pg booklet chronicles a company's array-processor software routines. It lists, in tabular form, the functions, mnemonics, and timings for the scientific subroutine library, Fortran intrinsics, and the host-support library. The brochure catalogs approximately 400 programs, including algorithms for signal processing, matrix arithmetic, vector operations, scalar operations, image processing, and Eispac functions.

CSPI, 40 Linnell Circle, Billerica, MA 01821.

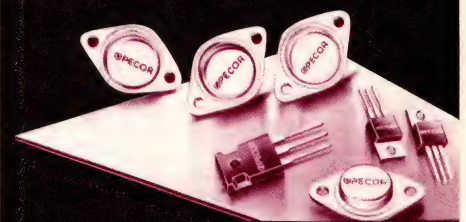
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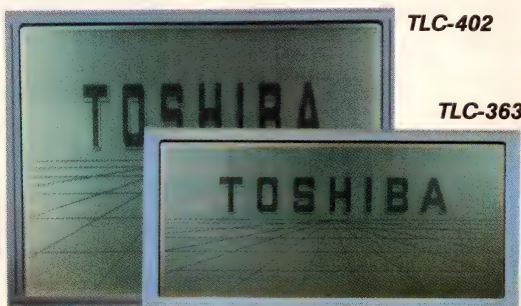
Simulated picture

New LCD modules from TOSHIBA give you 640×200 dot displays plus your choice of display area: virtually the size of an ordinary magazine or half that size.

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Specifications

	TLC-402	TLC-363
Display		
Number of Characters	80 $\times$ 25 (2,000 characters)	80 $\times$ 25 (2,000 characters)
Dot Format	8 $\times$ 8, alpha-numeric	8 $\times$ 8, alpha-numeric
Overall Dimensions (W $\times$ H $\times$ D)	274.8 $\times$ 240.6 $\times$ 15.0 mm	275.0 $\times$ 126.0 $\times$ 15.0 mm
Maximum Ratings		
Storage Temperature	-20 — 70°C	-20 — 70°C
Operating Temperature	0 — 50°C	0 — 50°C
Supply Voltage	V _{DD}	7 V
	V _{DD} -V _{EE}	18 V
Input Voltage	0 $\leq$ V _{IN} $\leq$ V _{DD}	V _{SS} $\leq$ V _{IN} $\leq$ V _{DD}
Recommended Operating Conditions		
Supply Voltage	V _{DD}	5 $\pm$ 0.25 V
	V _{EE}	-13 V Max.
Input Voltage	High	4.0 V Min.
	Low	0.5 V Max.
Typical Characteristics (25°C)		
Response Time	Turn ON	300 ms
	Turn OFF	300 ms
Contrast Ratio	5	5
Viewing Angle	15 — 35 degrees	15 — 35 degrees

Design and specifications are subject to change without notice.

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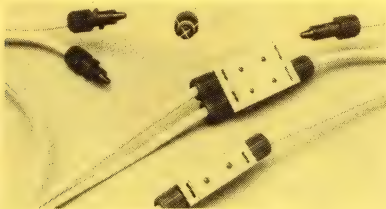
Toshiba (UK) Ltd.: Electronic Components Div., Toshiba House, Frimley Road, Frimley, Camberley, Surrey GU 165JJ, England Tel: 0276 62222

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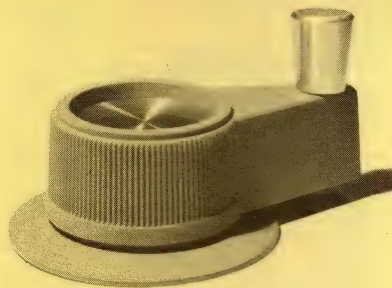
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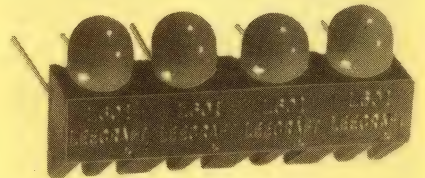
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CONTROL KNOBS

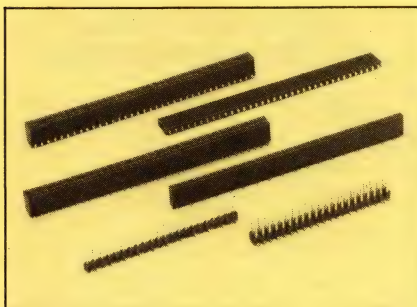
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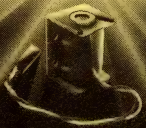
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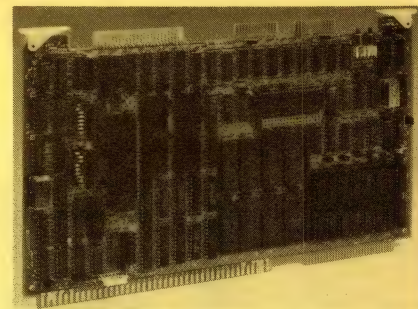
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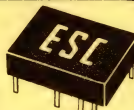
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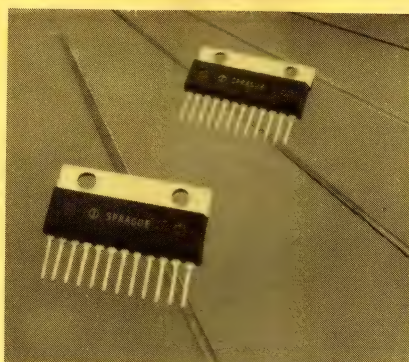
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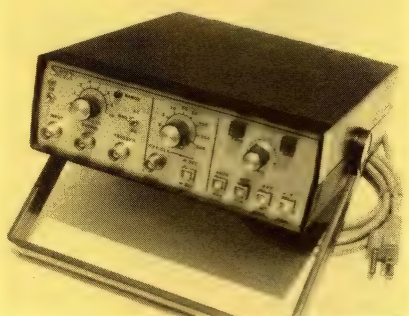
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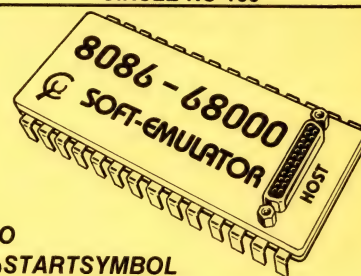
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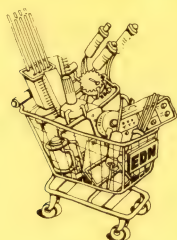
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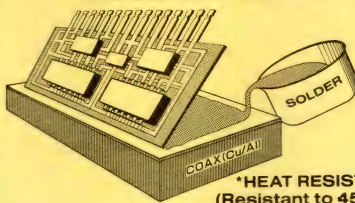
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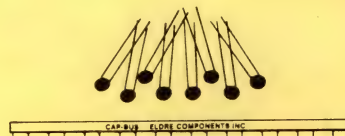
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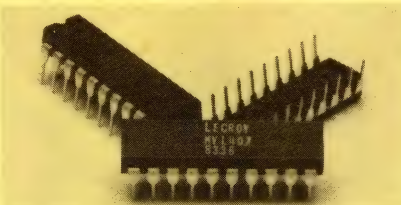
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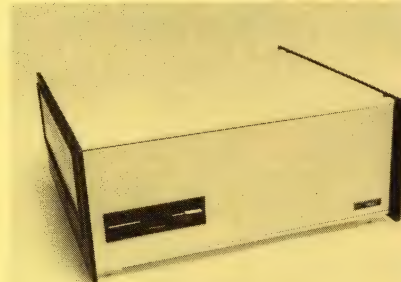
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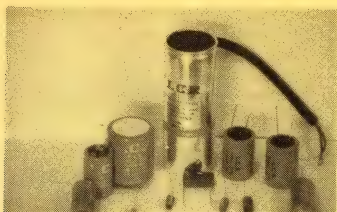
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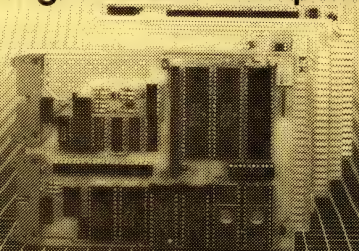


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NEW BOOKS

Marketing Technical Ideas and Products Successfully! 400 pgs; IEEE members, \$29.40; nonmembers, \$48.95; IEEE Press, New York, NY, 1985.

Intended to introduce technical personnel to the marketing process, this anthology is geared to the special needs of marketing technical products and ideas. The volume contains selected articles and papers from American, Canadian, and European magazines and journals, ranging from the development of a marketing program to ways to evaluate its effectiveness.

The 67 papers are divided into five parts: Industrial Marketing: An Overview, The Marketing Program, Marketing Methods, Producing Marketable Copy, and Measuring Program Effectiveness. Topics covered include the marketing responsibilities of the engineer and scientist, advertising-sales productivity and how to measure it, and the needs of the customer and client during product development.

How to Write Papers and Reports About Computer Technology, by Charles H Sides. 162 pgs; \$21.95 (hardcover), \$14.95 (paperback); ISI Press, Philadelphia, PA, 1985.

This book is intended to assist computer professionals in writing effective proposals, documentation, specifications, reports, and papers. The guide focuses on such topics as writing a good user manual, defining your audience, writing proposals that work, and incorporating graphics into your writing. It also discusses which techniques work best for obtaining information during interviews.

Protecting Electronic Equipment from Electrostatic Discharge, by Edward A Lacy. 176 pgs; \$16.95 (hardcover), \$11.45 (paperback); TAB Books Inc, Blue Ridge Summit, PA, 1984.

This book describes precautions and solutions for minimizing ESD damage. It presents information on how to choose electrostatic test equipment, techniques for handling semiconductors, how to select the proper air ionizer, and techniques for protecting semiconductors during shipment and storage. The book also offers suggestions on how to use tools around semiconductors, what to consider when selecting grounded wrist straps and protective clothing, how to use humidity control effectively, techniques for building a static-free workstation, and methods for implementing ESD-control techniques in the field.

Flat-Panel Displays and CRTs, edited by Lawrence E Tannas Jr. 488 pgs; \$52.50; Van Nostrand Reinhold, New York, NY, 1984.

This anthology presents up-to-date coverage of flat-panel display technologies and their emerging relationship with CRTs. Contributing experts examine the display-system requirements, performance measures, and technical capabilities of both flat-panel displays and CRTs.

The book covers the theory of operation, device technology, materials, processes, and configurations for CRTs, electroluminescent displays, plasma displays, LEDs, and LCDs. The characterization of each type of display will help you select the appropriate technology for your application.

A User Guide to the UNIX System, 2nd edition, by Dr Rebecca Thomas and Jean Yates. 716 pgs; \$18.95; Osborne McGraw-Hill, Berkeley, CA; 1985.

Unlike the first edition, this book places greater emphasis on the concepts that underlie the Unix system and the character of the system as a whole. It isolates a core of information that everyone needs to know in order to use the Unix system effectively.

Divided into four parts, the book is useful as a reference as well as a source for more advanced study. Part 1 provides an overview of the Unix system and describes the programs' applications for business and science. Part 2 teaches you fundamental concepts and procedures as well as special features of the programs. Part 3 discusses 44 of the more useful command programs in detail, and part 4 provides additional information in seven appendices.

Gate Array and Standard Cell IC Vendor Directory, by Source III Inc. 385 pgs; \$195; Electronic Trend Publications, Cupertino, CA, 1984.

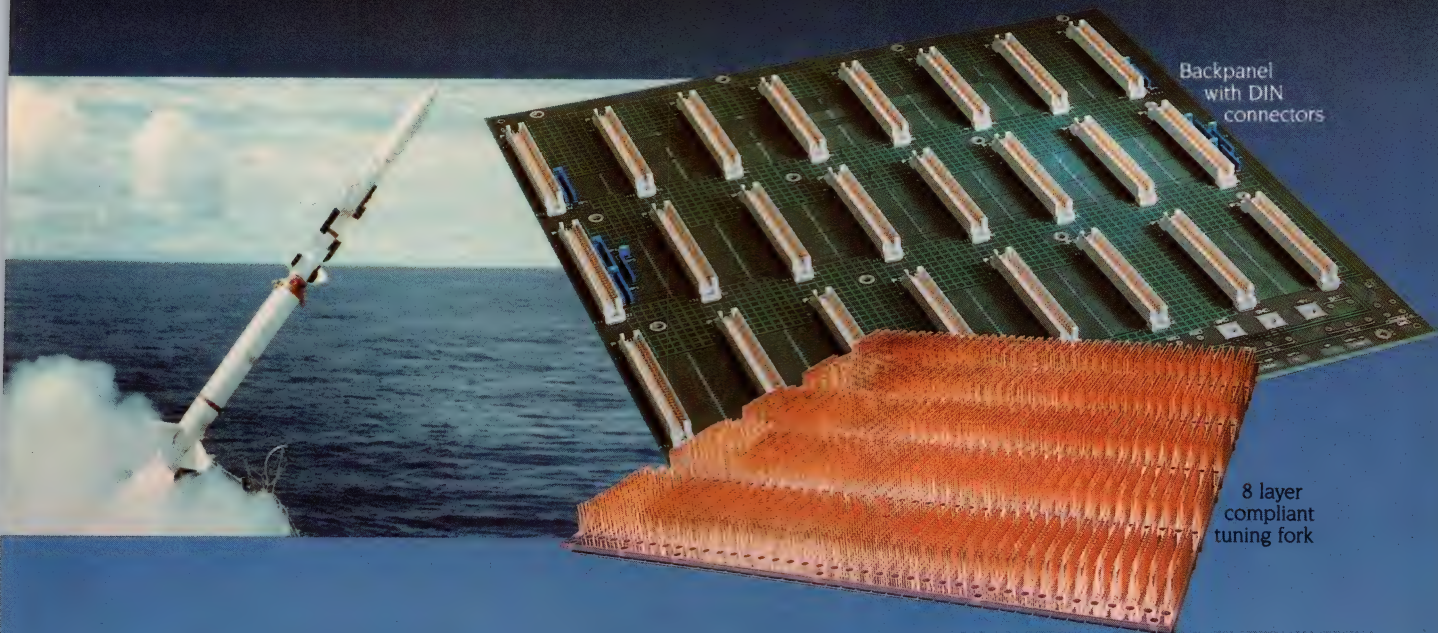
This guide provides the designer or procurer of semicustom ICs with the information necessary for selecting specific vendors and parts. In addition, it covers the technology and vendor-interfaces for gate-array and standard-cell manufacturers. Company profiles include the following data: corporate background, semicustom experience, development processes, production time, and CAD information.

Industrial Materials Science and Engineering, edited by Lawrence E Murr. 616 pgs; \$69.75; Marcel Dekker Inc, New York, NY; 1984.

This book gives an overview of current materials properties and behavior, provides a historical perspective, and discusses the emerging materials technologies. The compendium covers such topics as generic materials categories, including metals, semiconductors, ceramics, and polymers; the role of microstructure in new materials development; surface phenomena (eg, films, coatings, surface modification, wear, and degradation); and materials characterization tools. In addition, the book includes illustrations, references, and discussions of problems and solutions reinforcing materials science applications and engineering principles.

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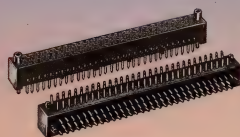
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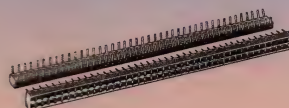
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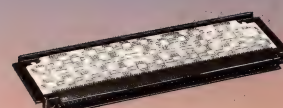
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THE NEXT GENERATION



PROFESSIONAL ISSUES

WRITTEN BY DEBORAH ASBRAND

NSF research centers open with high hopes for innovative technology, better-trained EEs

The National Science Foundation's funding of six engineering research centers at US universities has touched off new levels of enthusiasm in both the education and industry sectors, rekindling hopes for US advancements in research and development and consequently in the international market. The centers began operating on May 1 and are conducting research in robotics, telecommunications, systems engineering (including VLSI circuits, CAE, and artificial intelligence), intelligent manufacturing systems, composites manufacturing, and biotechnology process engineering.

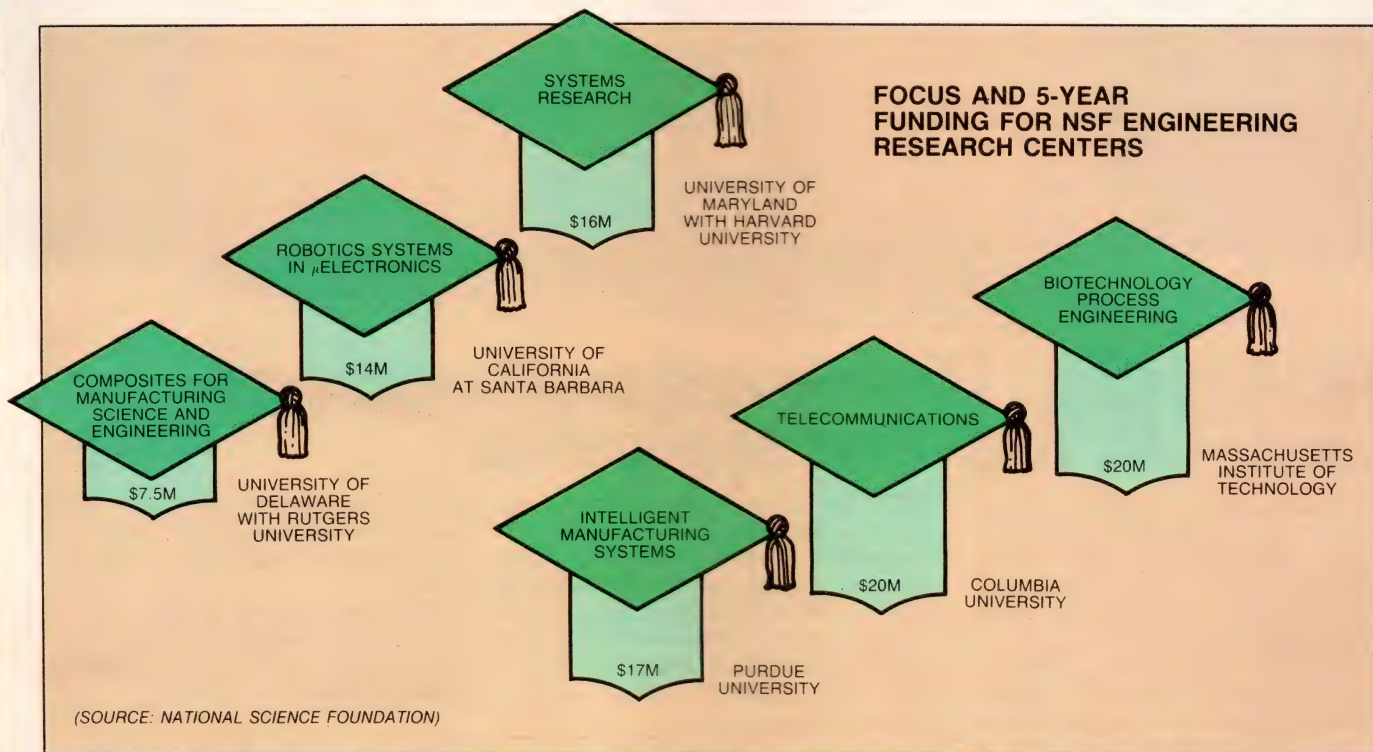
"The basic idea behind this new program is to help university researchers develop long-term, fundamental knowledge of engineering problems of significance to indus-

try, and to educate a new generation of students who can readily integrate ideas and techniques from a wide range of scientific and engineering disciplines," NSF director Erich Bloch said when the funding awards were announced in April. In addition, the centers provide a research component that has been noticeably lacking in undergraduate engineering education.

Institutions sharing the NSF's initial \$9.5 million in funding are the University of California at Santa Barbara (UCSB), Columbia University, University of Delaware, University of Maryland, Massachusetts Institute of Technology, and Purdue University. The University of Delaware will operate its center in conjunction with Rutgers University; the University of Maryland will op-

erate in collaboration with Harvard University. The research sites were selected from 142 submissions received by the NSF after it announced the program last year. They will receive a total of \$94.5 million in NSF funding over the next five years.

The research centers are the result of the NSF's recent reorganization of its Engineering Directorate (see EDN, May 2, pg 311). The NSF expects that the federal funding will begin a healthy collaboration between industry and education, with the private sector eventually taking on a more substantive role in financing the centers and participating in research. Susan Hackwood, director of the Center for Robotics Systems in Microelectronics at UCSB, says industry support for the center has



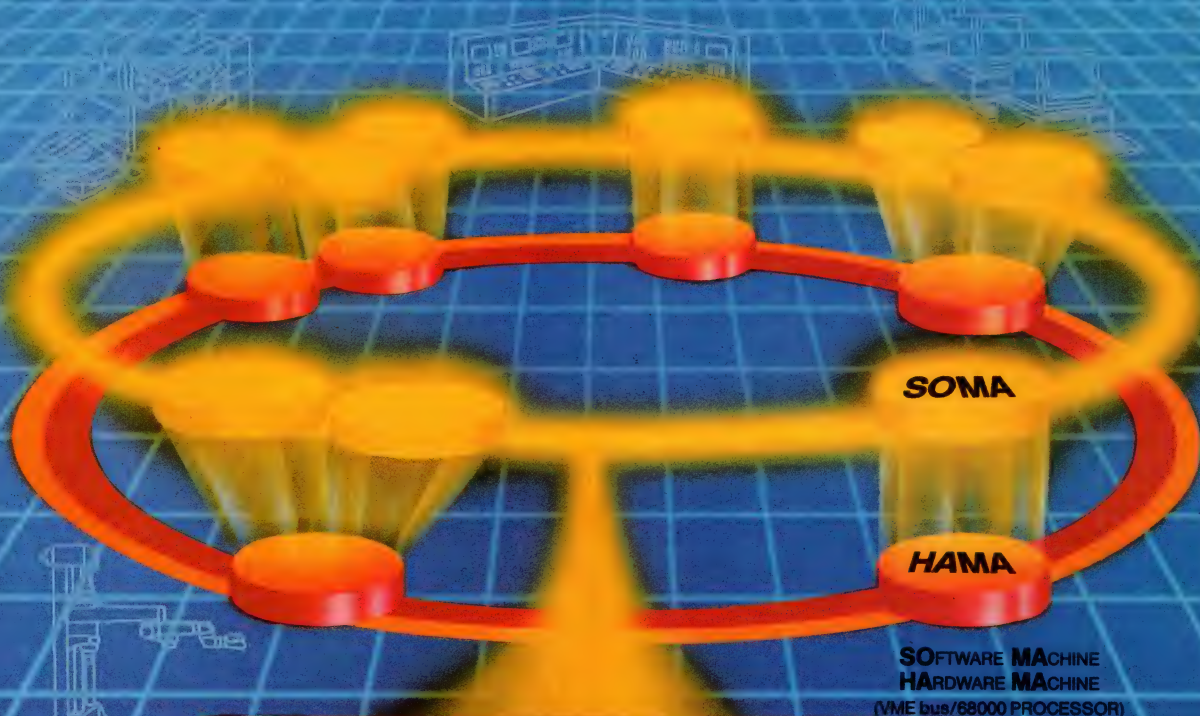
The National Science Foundation (NSF) chose these six engineering research centers for \$94.5 million in funding over the next five years. The NSF expects the funding to begin a healthy collaboration between industry and education.



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CIRCLE NO 137

PROFESSIONAL ISSUES

been enthusiastic from the start. Intel chairman Gordon Moore was impressed enough by the UCSB center's plans to voice his support during the site review the university underwent as a grant finalist. A wide base of support from industry was also evidenced at the University of Maryland, where a dozen industry representatives attended the NSF review.

At Columbia University, Mischa Schwartz, director of the NSF-funded Center for Telecommunications Research, is working to foster liaisons between the university and nearby companies, which are "some of the biggest telecommunications manufacturers, carriers, and users in the world," he says. The center's research will focus on developing integrated telecommunications networks capable of carrying such disparate types of traffic as data, voice, and video. He hopes to have telecommunications professionals lecture, conduct seminars, and work in

the center with faculty or students on projects one or two days each week. In the future, he hopes to work with Columbia's School of Law and School of International Affairs to incorporate the study of telecommunications law and regulatory policies into the center's curriculum.

But more than advancing research and development, the centers have restored the badly needed research component to undergraduate engineering education. A report issued in July 1983 by National Academy of Engineering president Robert White had cited sparse research opportunities as a glaring weakness in US undergraduate training of engineers. Most educators see the educational element of the research centers as the program's greatest strength.

"One of the problems universities have is that they have no in-house problems to work on," says William Dick, deputy director of the University of Delaware's Center for Com-

posites for Manufacturing Science and Engineering. "Students need problems to address. One of the benefits of working with industry is that [industry has] the problems we can train our students with, and that is both to the students' and industry's advantage."

"The university needs industry as much as, if not more than, industry needs the university," says UCSB's Hackwood. At that college, 150 to 200 undergraduates will use the center's facilities, including the center's 1400-sq-ft Class 100 clean room. Three undergraduate courses will have laboratories associated with the robotics center. Hackwood, a professor of electrical engineering, says students will be working to design and build robotics systems for microelectronic-device manufacturing. "What's unique about this center is the focus on systems work, which means building a whole working system, rather than just playing with one robot. It

NAE takes steps to boost US competitiveness

The National Academy of Engineering is another organization that has set its sights on using US technology to tackle the difficulties of competing in the international market. It established seven new programs to accomplish its goals of assessing the nation's technical needs, strengthening engineering education, and promoting national awareness of the importance of technical leadership. The new goals are part of the academy's Decade III Program Plan, a 10-year agenda that the NAE approved last year.

After a year of evaluation and planning, the NAE decided to step up its participation in the advancement of the US's technological leadership by establishing programs to study:

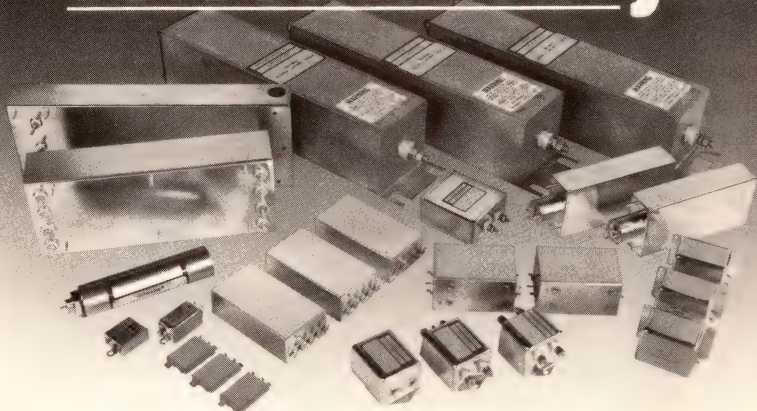
- Industrial issues
- Engineering education
- The status of technology and engineering research
- Technology and society
- Public awareness
- International issues
- Management support.

The Decade III Program Plan will be funded by

donations from the private sector; the NAE hopes to raise \$30 million for the program in the next few years. The organization plans to devote the most funds to the study of international issues, (including cooperative relationships with the Peoples' Republic of China), nuclear safeguards, and global technologies. Engineering education is earmarked as the second financial priority and will encompass future educational needs, the fundamental structure of engineering education, and the establishment of a database for engineering and technology studies.

The NAE is a private organization established in 1964 to study science and technology issues. It is the engineering counterpart to the National Academy of Sciences (NAS). More than 1200 engineers from industry, education, and research and development are honorary members of the NAE. The NAE, NAS, and the Institute of Medicine operate under the auspices of the National Research Council, which carries out more than 300 studies each year for a variety of sponsors from industry and government.

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means doing something useful with the robots," says Hackwood. Her goal is to see robotics become a "sound academic discipline," and she envisions the center in a few years developing robots for oceanographic and space applications.

Students at the University of Maryland's Center on Systems Research will study the implications and applications of CAE, VLSI circuits, and artificial intelligence on design methodologies. "Currently used methods and theories for the design of control and communications systems were really motivated and thought out on the basis of a different implementation," says the center's director, John Baras, a professor of electrical engineering. "Now the technology has changed drastically, but the corresponding design theories and methodologies have not. We are in an era where we can no longer afford to separate the design processes from the way we're going to implement the design." Baras says that students will participate in each of the center's projects and will also have the opportunity to attend seminars on various projects. He expects 50 undergraduate and 70 graduate students to participate in the center's activities.

Columbia University's Schwartz says students will play a big role in the school's telecommunications research, and he expects to have 200 undergraduates participating in research with 200 graduate students. Daniel Wang, director of MIT's Center on Biotechnology Process Engineering, is confident that the exposure to research provided by the centers to undergraduate students will contribute to "a new breed of professionals."

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Aug. 8	July 16	Display Technology Technical Article Database Index Instrumentation	
Aug. 22	July 30	Military Electronics Special Issue High Speed ICs Power Supplies Software Semicustom ICs	Closing 8/20 Mailing 8/27
Sept. 5	Aug. 13	Power Semiconductors Computer Peripherals Components CAE Report	

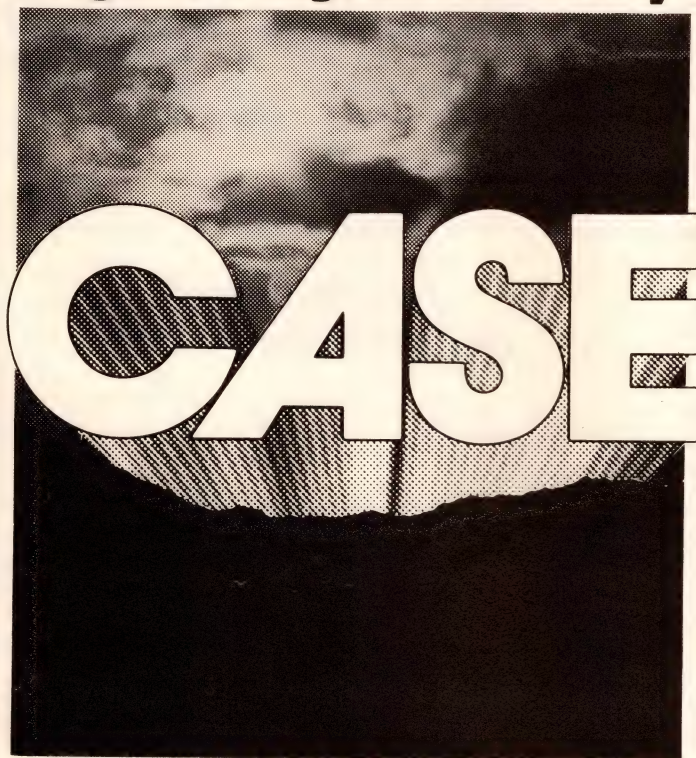
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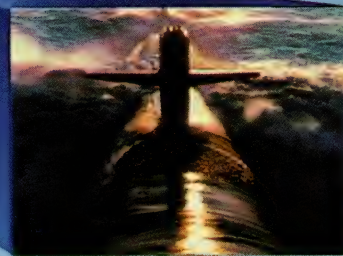
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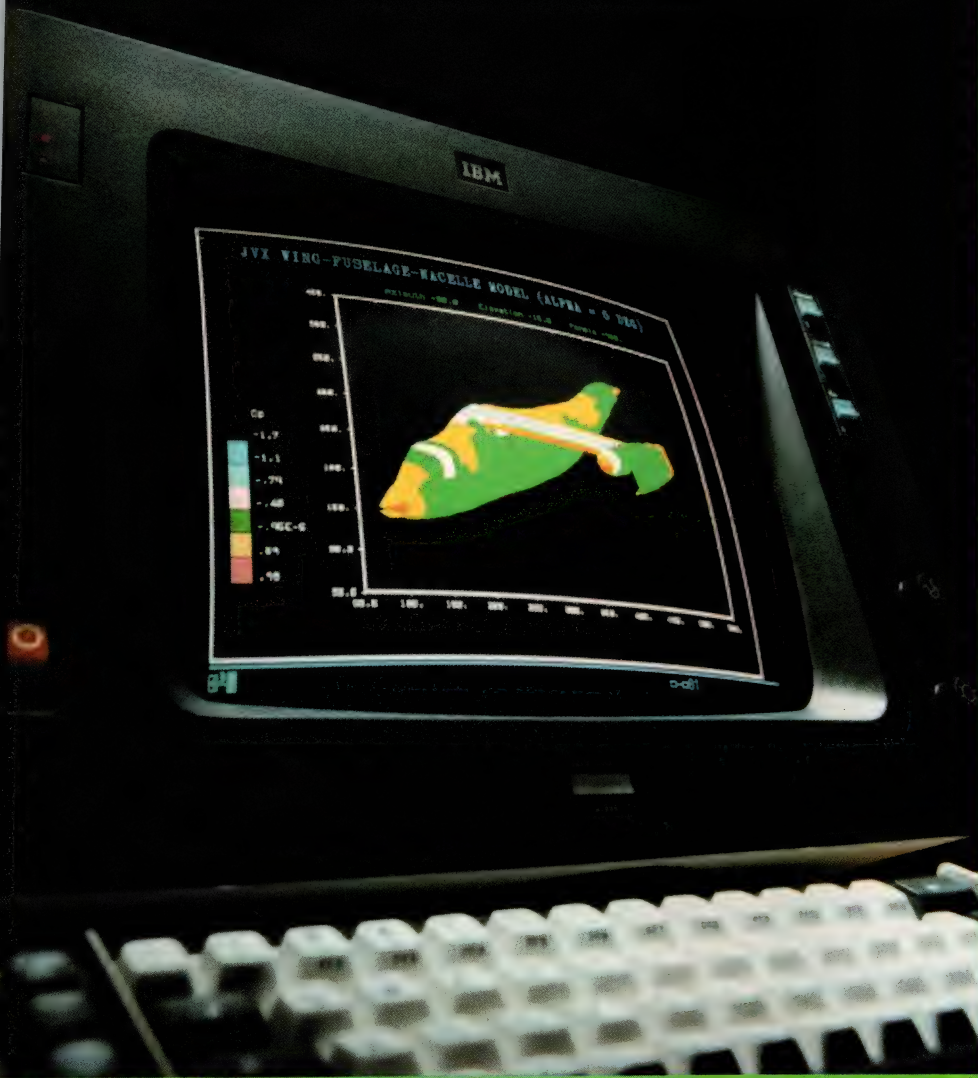
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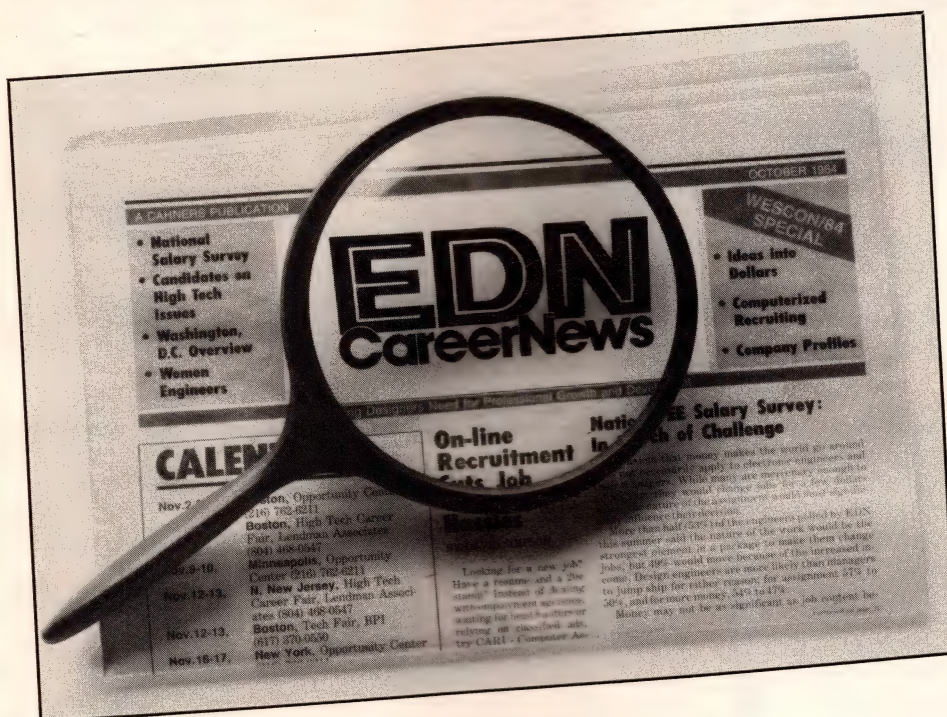
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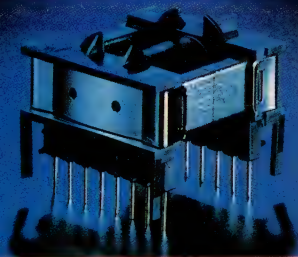
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CIRCLE NO 141

LOOKING AHEAD

EDITED BY GEORGE STUBBS

Voice/data terminal sales to reach \$650M in '87

Terminals that integrate voice and data communications and data processing—equipment which until recently has been considered sophisticated playthings for executives—are about to achieve the level of popularity long predicted for them. The market for these terminals will grow from 1984's modest \$53 million to \$650 million in 1987, forecasts Market Intelligence Research Co (Palo Alto, CA).

This explosive sales growth will be the result of a change in customer base and the introduction of integrated voice/data microcomputers by such formidable companies as AT&T Information Systems and IBM. The most recent products have been designed for middle managers and other employees who must manipulate and move large amounts of information. These workers need local-processing capabilities and advanced telephone, data-query, and time-management features.

In terms of meeting these needs, integrated voice/data terminals mesh logically with several emerging trends in the datacomm and telecomm fields: Vendors of digital PBXs, electronic-mail packages, public and private databases, and videotex/teletext systems will strive to exploit the capabilities of the integrated terminals. Some of these companies may even offer voice/data terminals of their own. Additional players in this market, besides AT&T and IBM, will include other manufacturers of terminals, microcomputers, personal computers, and complete datacomm/telecomm systems.

According to Brian Jeffery, research director of the International Technology Group (Palo Alto, CA), the integrated voice/data terminal constitutes a useful enhancement to the existing personal-computer workplace. In fact, Market Intelli-

gence Research predicts that integrated microcomputers could compose as much as 10 to 12% of the personal-computer market by 1989.

Motion-control market to double in Europe by '89

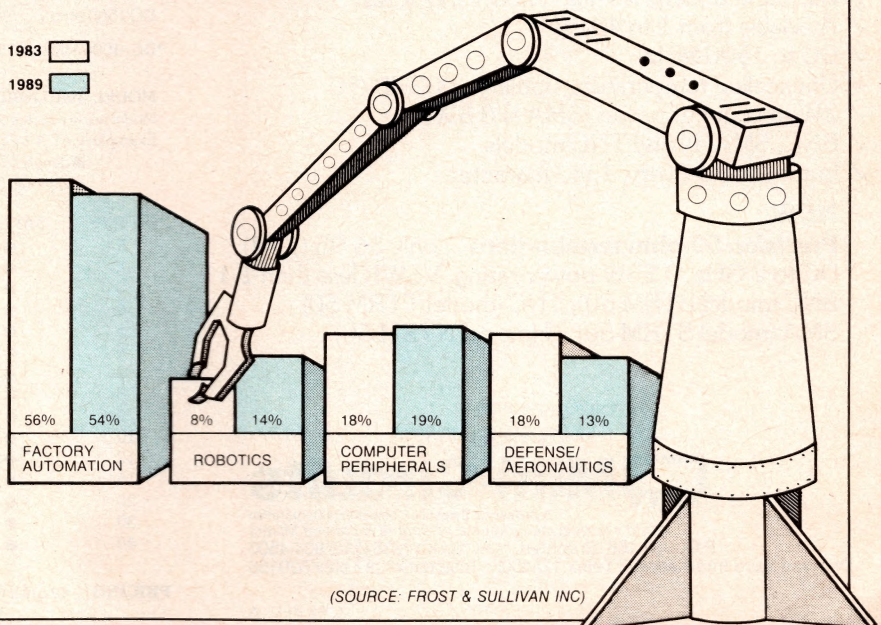
The small motors, drives, and control devices used in robots, disk drives, and other products that require rapid and precise movements for proper performance constitute a large and growing market. In Western Europe, the average annual growth rate for such products will be 15.5%, increasing from \$900 million in 1983 to \$2 billion in 1989, according to the market-research firm Frost & Sullivan Inc (New York, NY).

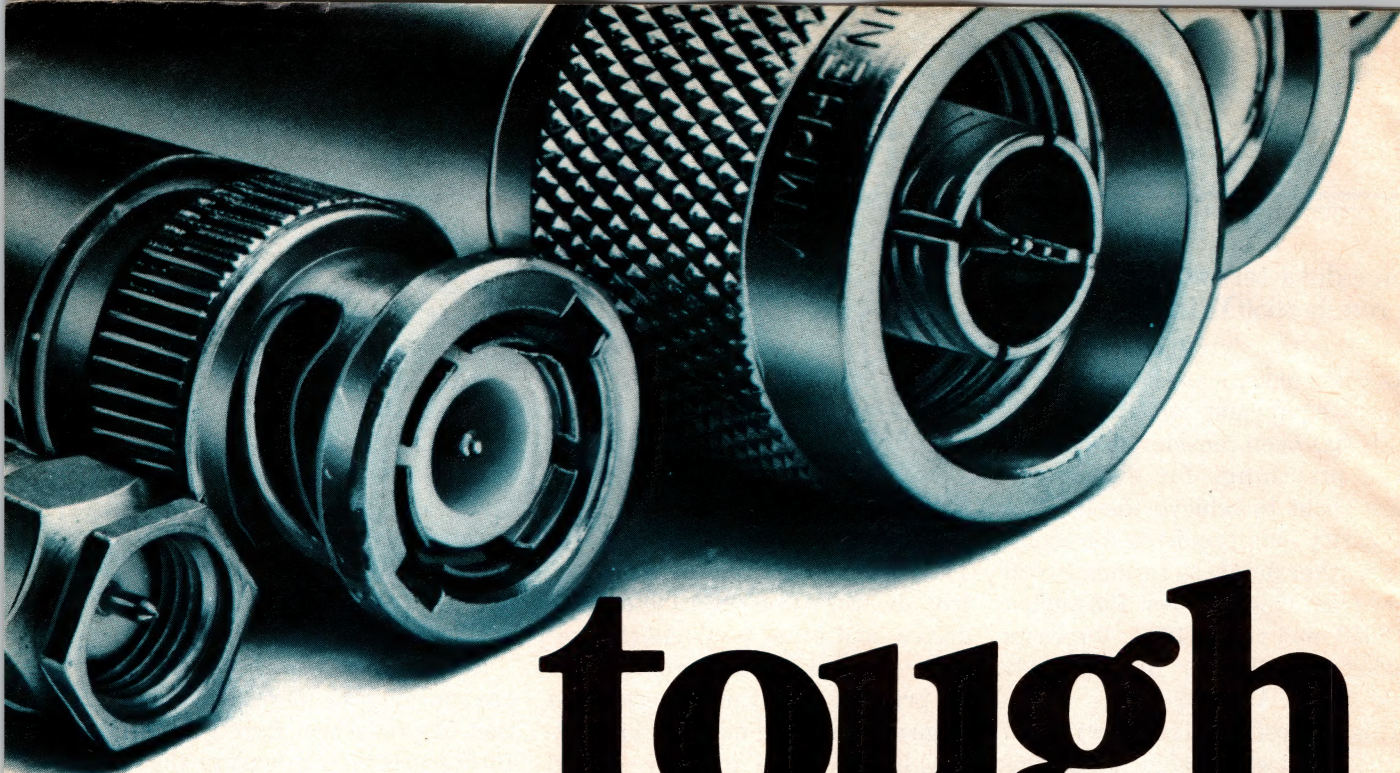
West German makers of the devices are expected to maintain their market dominance through 1989. Their 37% market share in 1983 will grow to 40% by 1989, Frost & Sullivan predicts. French vendors will collectively establish themselves as the number two makers of motion-control products.

Factory automation has been the driving force behind this market surge, and it will continue in that role through at least the next four years. Robotics is the fastest growing application area for the devices. The use of motion-control parts in computers and peripherals will hold steady throughout the 1983-89 period, while their use in defense/aeronautics applications will decline in comparison to these other areas.

Several technological advances are spurring the increasing automation of production facilities. Intel's Bitbus promises to ensure that the various parts and departments of the automated factory will be able to work with one another. Matsushita's (Japan) wound-type flat motor provides extremely accurate control in the start/stop and speed-control functions of machine tools, welding machines, card readers, line printers, data-recording devices, and other products. Last but not least, SGS-Ates (Italy) has developed a 2-chip motor-control system that might replace the handful of ICs and power transistors needed to drive a stepper motor from a μ P.

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3	●	■	●	●
4	●			
5	●			
6	●	■	●	●
7	●			
8	●			
9	●			
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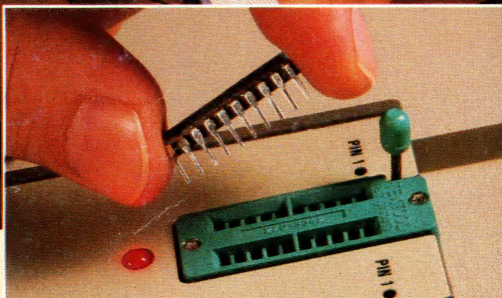
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